# **CDA 6214-001: Structure VLSI Design**

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## Code generation, compilation, and schematics

We utilize Logisim simulation software to create a high-level Verilog code, and for timing simulation and verification of the generated code, we leverage Intel QuartusTM combined with ModelSimTM.

## Design diagram

Logisim is a graphical design tool that allows users to manually layout each gate and wire, converting the design into Verilog code internally. This software is widely utilized in the VLSI industry for both educational and instructional purposes.

Here's a representation of a schematic created in Logisim:

Inputs: Marked with the color "BLUE."

Outputs: Indicated by the color "RED."

Single Wires: Represented by the color "GREEN."

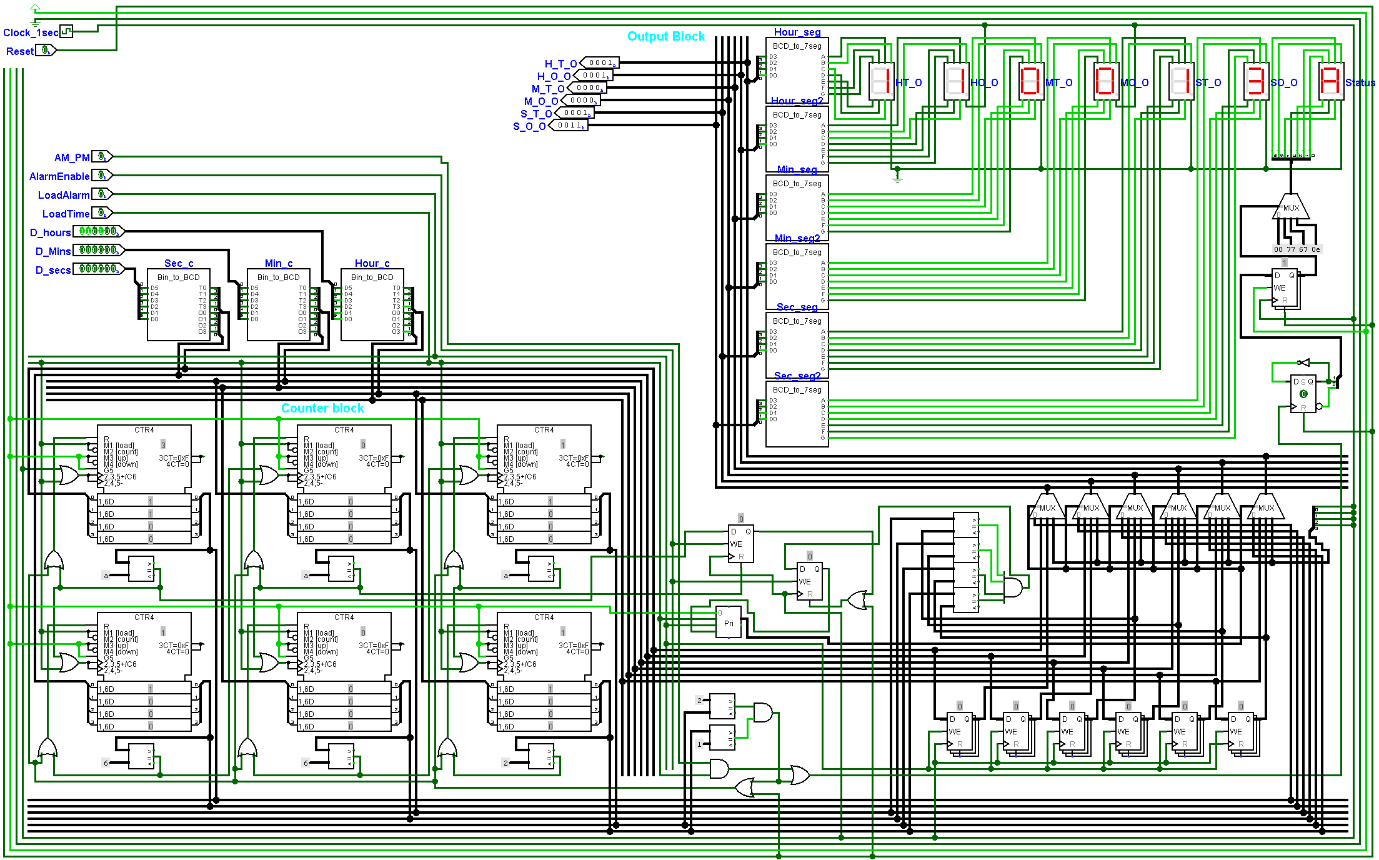
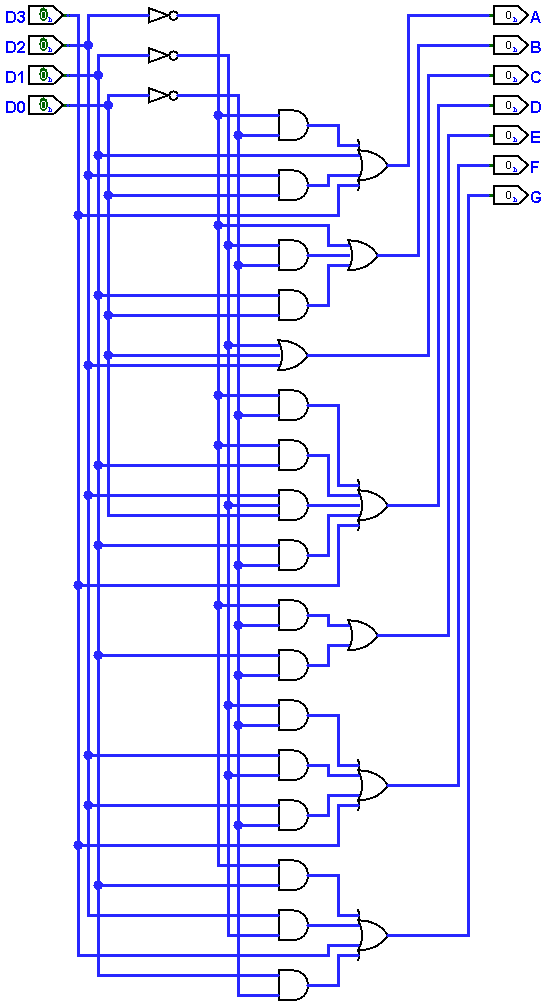
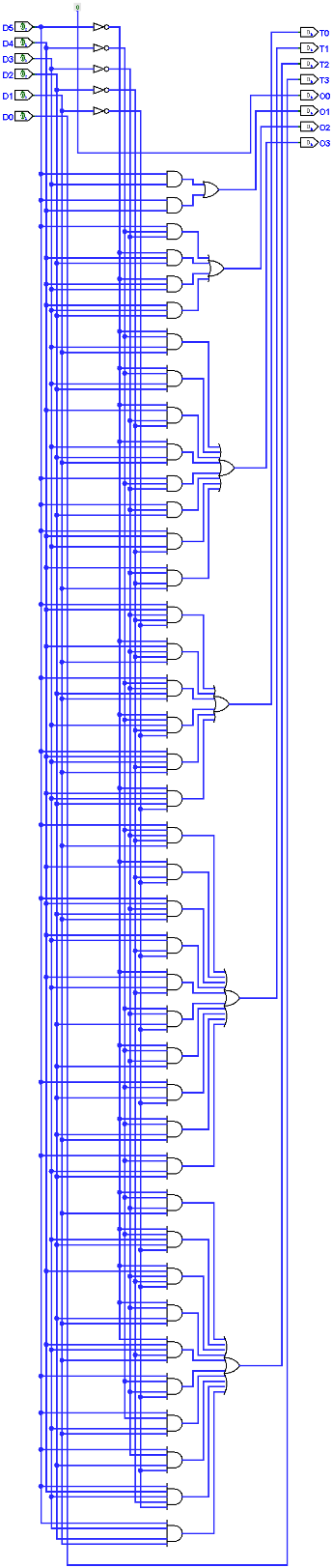
Busses: Displayed in the color "BLACK."  


Fig 1 : Logisim design simulation with wiring counters and diagram

  
Fig 2: BCD to 7 segment display

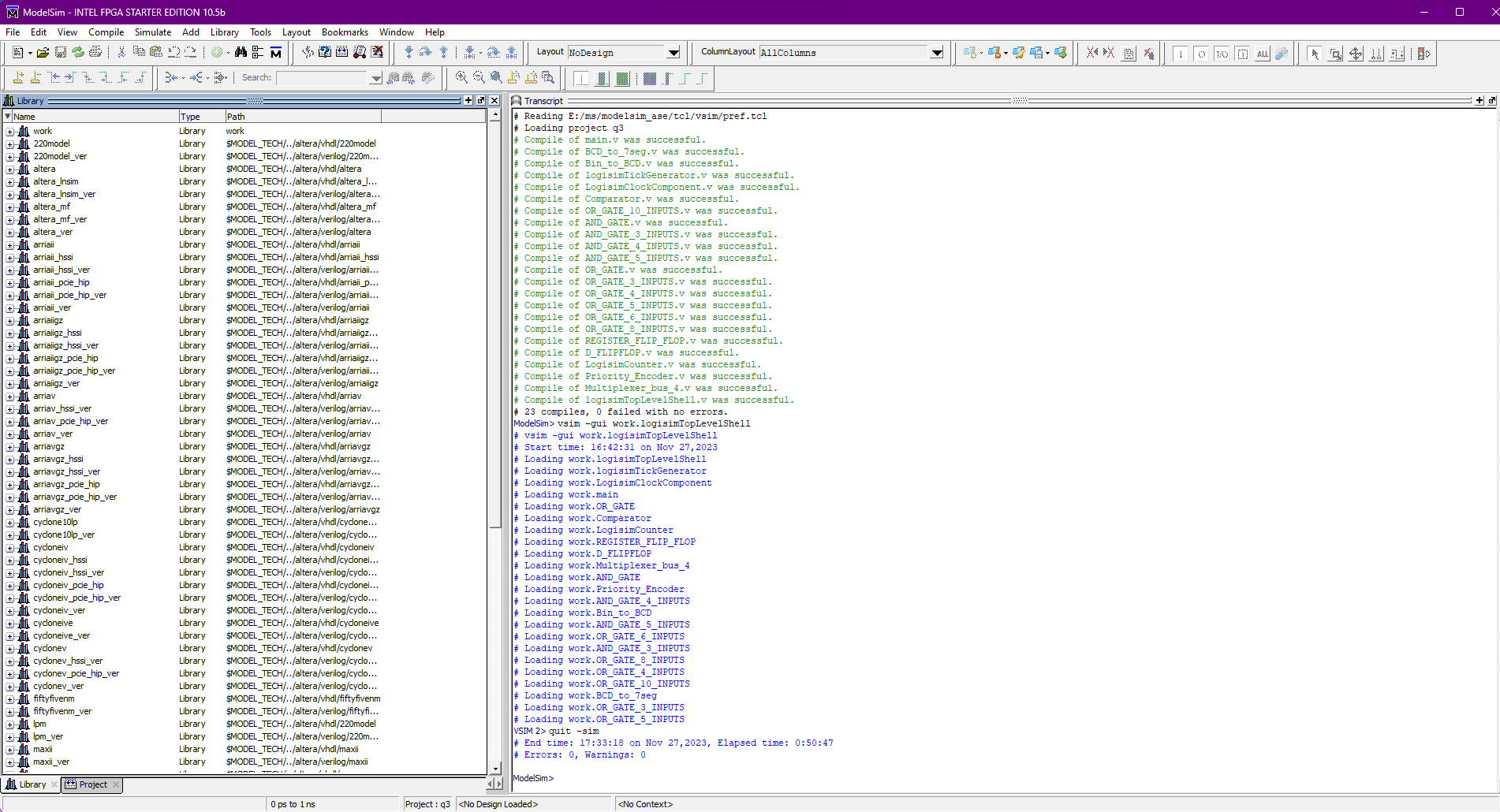
  
Fig 3 : 6 bit binary to BCD

## Code Compilation and Simulation testing

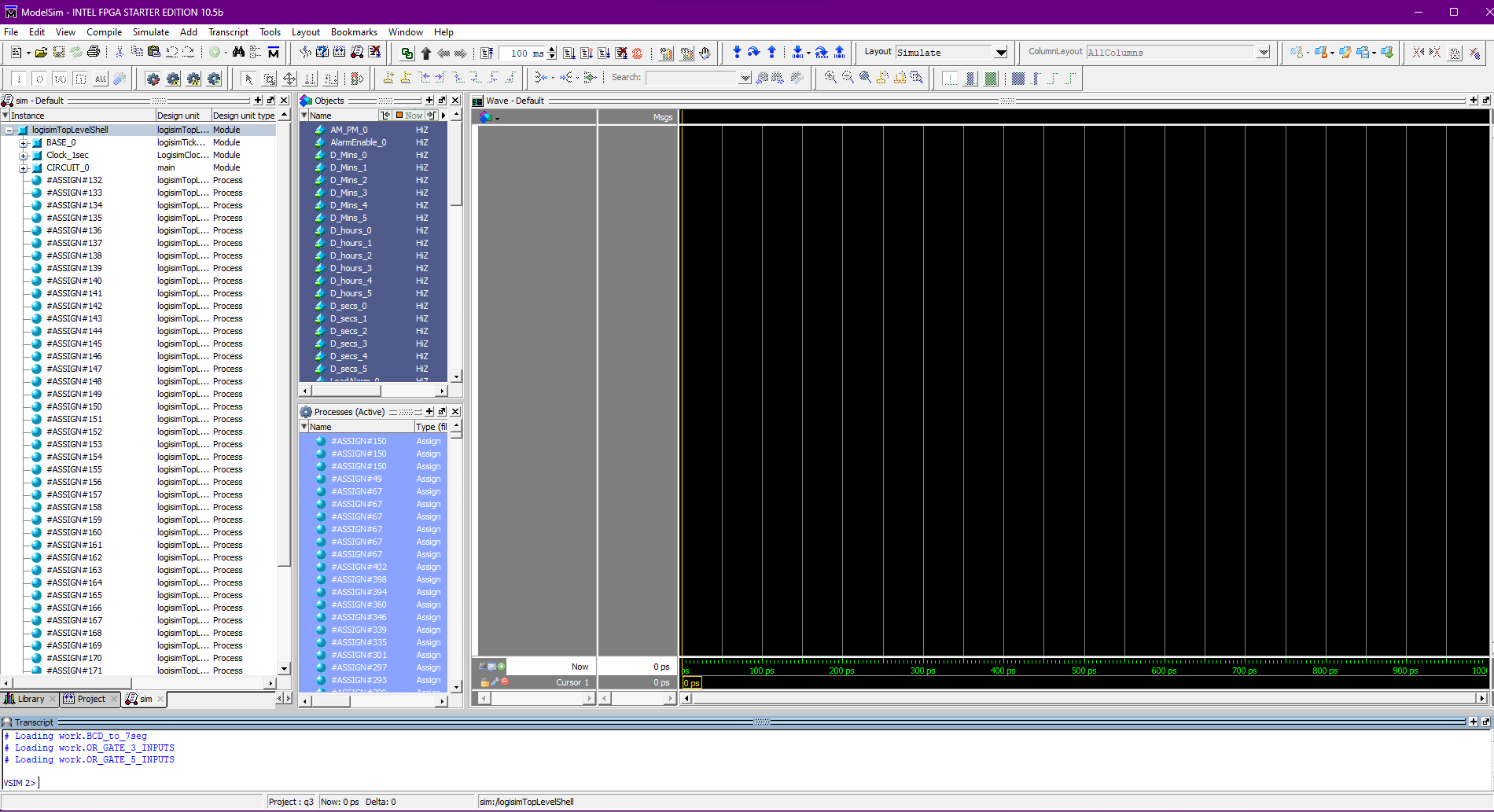
The code produced by Logisim undergoes inspection, and optimizations are applied using ModelSim.

## Code compilation success

The code below has been successfully compiled and is prepared for utilization in any FPGA equipped with 7-segment displays. It includes inputs for entering, loading time, and managing alarms.



## Simulation begin success

To guarantee consistency with Logisim, we verify whether the simulation has been loaded correctly within ModelSim.

## Timing Diagram

The timing diagram is shown below covering various scenarios A screenshot of a computer

Description automatically generated

Fig 1 : Reflecting output in modelsim for time load and alarm load  
A screenshot of a computer

Description automatically generated

Fig 2 : Reflecting output for alarm ring

A screenshot of a computer

Description automatically generated

Fig 3: Reflecting diagram for loading of timeA screenshot of a computer

Description automatically generated

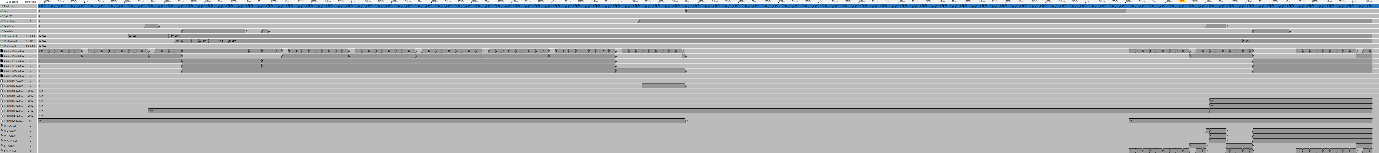
Fig 4 : reflecting diagram for general timing of clock ( notice fpga global clock runs faster since every global 256 clocks is 1 second clock )  


Fig 5 : Time load and alarm load on begin

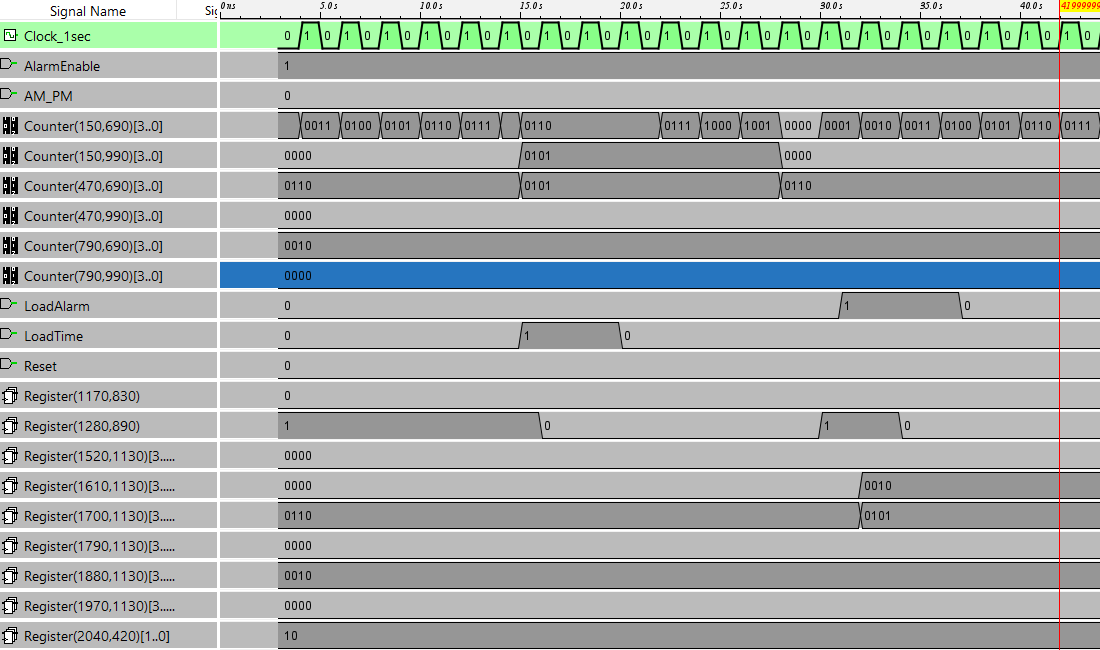


Fig 6 : Time load while running

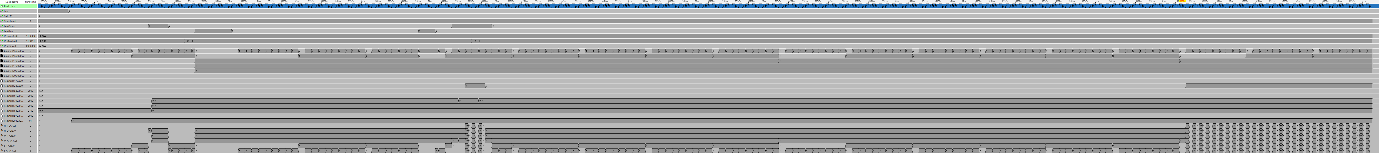


Fig 7: initial alarm to remind set time and actual alarm ring begin



Fig 8: Alarm Ring begin and end (alarm ringing for 1 minute )

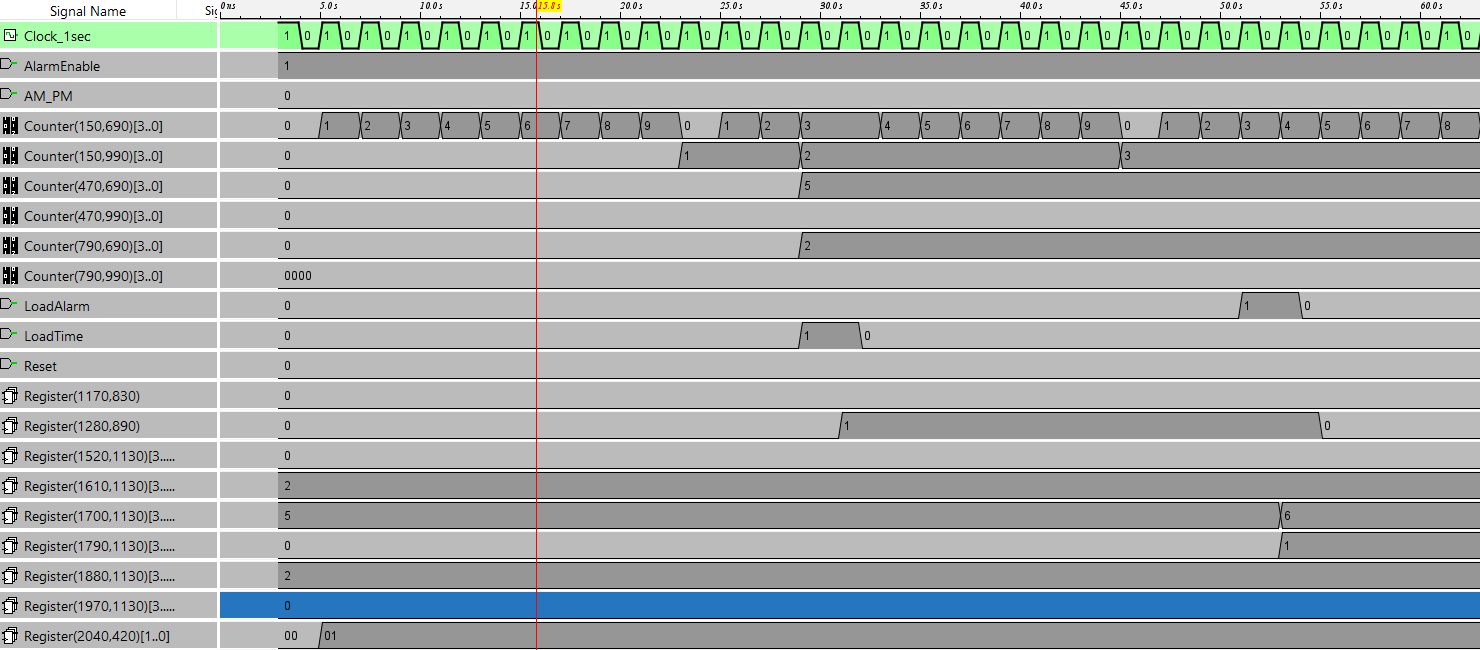


Fig 9 : Time start from zero with alarm disabled



Fig 10 : Time running and changing every 59 seconds and every 59 minutes with AM/PM toggle every 12 hours

## Code

* main.v

**module** main**(** AM\_PM**,**

AlarmEnable**,**

D\_Mins**,**

D\_hours**,**

D\_secs**,**

LoadAlarm**,**

LoadTime**,**

Reset**,**

logisimClockTree0**,**

logisimOutputBubbles **);**

\*\* The inputs are defined here \*\*

**input** AM\_PM**;**

**input** AlarmEnable**;**

**input** **[**5**:**0**]** D\_Mins**;**

**input** **[**5**:**0**]** D\_hours**;**

**input** **[**5**:**0**]** D\_secs**;**

**input** LoadAlarm**;**

**input** LoadTime**;**

**input** Reset**;**

**input** **[**4**:**0**]** logisimClockTree0**;**

\*\* The outputs are defined here \*\*

**output** **[**55**:**0**]** logisimOutputBubbles**;**

\*\* The wires are defined here \*\*

**wire** **[**3**:**0**]** s\_logisimBus0**;**

**wire** **[**5**:**0**]** s\_logisimBus106**;**

**wire** **[**1**:**0**]** s\_logisimBus109**;**

**wire** **[**5**:**0**]** s\_logisimBus110**;**

**wire** **[**3**:**0**]** s\_logisimBus111**;**

**wire** **[**6**:**0**]** s\_logisimBus116**;**

**wire** **[**6**:**0**]** s\_logisimBus120**;**

**wire** **[**3**:**0**]** s\_logisimBus127**;**

**wire** **[**3**:**0**]** s\_logisimBus128**;**

**wire** **[**3**:**0**]** s\_logisimBus129**;**

**wire** **[**6**:**0**]** s\_logisimBus130**;**

**wire** **[**3**:**0**]** s\_logisimBus133**;**

**wire** **[**3**:**0**]** s\_logisimBus15**;**

**wire** **[**1**:**0**]** s\_logisimBus17**;**

**wire** **[**3**:**0**]** s\_logisimBus19**;**

**wire** **[**3**:**0**]** s\_logisimBus2**;**

**wire** **[**3**:**0**]** s\_logisimBus20**;**

**wire** **[**3**:**0**]** s\_logisimBus23**;**

**wire** **[**3**:**0**]** s\_logisimBus25**;**

**wire** **[**3**:**0**]** s\_logisimBus26**;**

**wire** **[**3**:**0**]** s\_logisimBus27**;**

**wire** **[**3**:**0**]** s\_logisimBus32**;**

**wire** **[**3**:**0**]** s\_logisimBus34**;**

**wire** **[**3**:**0**]** s\_logisimBus36**;**

**wire** **[**3**:**0**]** s\_logisimBus37**;**

**wire** **[**3**:**0**]** s\_logisimBus4**;**

**wire** **[**5**:**0**]** s\_logisimBus42**;**

**wire** **[**3**:**0**]** s\_logisimBus43**;**

**wire** **[**3**:**0**]** s\_logisimBus49**;**

**wire** **[**3**:**0**]** s\_logisimBus51**;**

**wire** **[**3**:**0**]** s\_logisimBus54**;**

**wire** **[**1**:**0**]** s\_logisimBus56**;**

**wire** **[**3**:**0**]** s\_logisimBus59**;**

**wire** **[**3**:**0**]** s\_logisimBus6**;**

**wire** **[**6**:**0**]** s\_logisimBus60**;**

**wire** **[**3**:**0**]** s\_logisimBus62**;**

**wire** **[**3**:**0**]** s\_logisimBus68**;**

**wire** **[**3**:**0**]** s\_logisimBus79**;**

**wire** **[**3**:**0**]** s\_logisimBus80**;**

**wire** **[**3**:**0**]** s\_logisimBus85**;**

**wire** **[**3**:**0**]** s\_logisimBus86**;**

**wire** **[**3**:**0**]** s\_logisimBus89**;**

**wire** **[**3**:**0**]** s\_logisimBus92**;**

**wire** **[**6**:**0**]** s\_logisimBus99**;**

**wire** s\_logisimNet1**;**

**wire** s\_logisimNet10**;**

**wire** s\_logisimNet100**;**

**wire** s\_logisimNet101**;**

**wire** s\_logisimNet102**;**

**wire** s\_logisimNet103**;**

**wire** s\_logisimNet104**;**

**wire** s\_logisimNet105**;**

**wire** s\_logisimNet107**;**

**wire** s\_logisimNet108**;**

**wire** s\_logisimNet11**;**

**wire** s\_logisimNet112**;**

**wire** s\_logisimNet113**;**

**wire** s\_logisimNet114**;**

**wire** s\_logisimNet115**;**

**wire** s\_logisimNet117**;**

**wire** s\_logisimNet118**;**

**wire** s\_logisimNet119**;**

**wire** s\_logisimNet12**;**

**wire** s\_logisimNet121**;**

**wire** s\_logisimNet122**;**

**wire** s\_logisimNet123**;**

**wire** s\_logisimNet124**;**

**wire** s\_logisimNet125**;**

**wire** s\_logisimNet126**;**

**wire** s\_logisimNet13**;**

**wire** s\_logisimNet131**;**

**wire** s\_logisimNet132**;**

**wire** s\_logisimNet134**;**

**wire** s\_logisimNet135**;**

**wire** s\_logisimNet136**;**

**wire** s\_logisimNet137**;**

**wire** s\_logisimNet138**;**

**wire** s\_logisimNet139**;**

**wire** s\_logisimNet14**;**

**wire** s\_logisimNet140**;**

**wire** s\_logisimNet141**;**

**wire** s\_logisimNet142**;**

**wire** s\_logisimNet143**;**

**wire** s\_logisimNet144**;**

**wire** s\_logisimNet145**;**

**wire** s\_logisimNet146**;**

**wire** s\_logisimNet147**;**

**wire** s\_logisimNet148**;**

**wire** s\_logisimNet149**;**

**wire** s\_logisimNet150**;**

**wire** s\_logisimNet151**;**

**wire** s\_logisimNet152**;**

**wire** s\_logisimNet153**;**

**wire** s\_logisimNet154**;**

**wire** s\_logisimNet155**;**

**wire** s\_logisimNet156**;**

**wire** s\_logisimNet157**;**

**wire** s\_logisimNet158**;**

**wire** s\_logisimNet159**;**

**wire** s\_logisimNet16**;**

**wire** s\_logisimNet160**;**

**wire** s\_logisimNet161**;**

**wire** s\_logisimNet162**;**

**wire** s\_logisimNet163**;**

**wire** s\_logisimNet164**;**

**wire** s\_logisimNet165**;**

**wire** s\_logisimNet166**;**

**wire** s\_logisimNet167**;**

**wire** s\_logisimNet168**;**

**wire** s\_logisimNet169**;**

**wire** s\_logisimNet170**;**

**wire** s\_logisimNet171**;**

**wire** s\_logisimNet172**;**

**wire** s\_logisimNet173**;**

**wire** s\_logisimNet174**;**

**wire** s\_logisimNet175**;**

**wire** s\_logisimNet176**;**

**wire** s\_logisimNet177**;**

**wire** s\_logisimNet178**;**

**wire** s\_logisimNet179**;**

**wire** s\_logisimNet18**;**

**wire** s\_logisimNet180**;**

**wire** s\_logisimNet181**;**

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**wire** s\_logisimNet184**;**

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**wire** s\_logisimNet202**;**

**wire** s\_logisimNet21**;**

**wire** s\_logisimNet22**;**

**wire** s\_logisimNet24**;**

**wire** s\_logisimNet28**;**

**wire** s\_logisimNet29**;**

**wire** s\_logisimNet3**;**

**wire** s\_logisimNet30**;**

**wire** s\_logisimNet31**;**

**wire** s\_logisimNet33**;**

**wire** s\_logisimNet35**;**

**wire** s\_logisimNet38**;**

**wire** s\_logisimNet39**;**

**wire** s\_logisimNet40**;**

**wire** s\_logisimNet41**;**

**wire** s\_logisimNet44**;**

**wire** s\_logisimNet45**;**

**wire** s\_logisimNet46**;**

**wire** s\_logisimNet47**;**

**wire** s\_logisimNet48**;**

**wire** s\_logisimNet5**;**

**wire** s\_logisimNet50**;**

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**wire** s\_logisimNet57**;**

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**wire** s\_logisimNet64**;**

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**wire** s\_logisimNet66**;**

**wire** s\_logisimNet67**;**

**wire** s\_logisimNet69**;**

**wire** s\_logisimNet7**;**

**wire** s\_logisimNet70**;**

**wire** s\_logisimNet71**;**

**wire** s\_logisimNet72**;**

**wire** s\_logisimNet73**;**

**wire** s\_logisimNet74**;**

**wire** s\_logisimNet75**;**

**wire** s\_logisimNet76**;**

**wire** s\_logisimNet77**;**

**wire** s\_logisimNet78**;**

**wire** s\_logisimNet8**;**

**wire** s\_logisimNet81**;**

**wire** s\_logisimNet82**;**

**wire** s\_logisimNet83**;**

**wire** s\_logisimNet84**;**

**wire** s\_logisimNet87**;**

**wire** s\_logisimNet88**;**

**wire** s\_logisimNet9**;**

**wire** s\_logisimNet90**;**

**wire** s\_logisimNet91**;**

**wire** s\_logisimNet93**;**

**wire** s\_logisimNet94**;**

**wire** s\_logisimNet95**;**

**wire** s\_logisimNet96**;**

**wire** s\_logisimNet97**;**

**wire** s\_logisimNet98**;**

\*\* The module functionality is described here \*\*

\*\* All clock generator connections are defined here \*\*

**assign** s\_logisimNet1 **=** logisimClockTree0**[**0**];**

\*\* Here all wiring is defined \*\*

**assign** s\_logisimBus62**[**0**]** **=** s\_logisimNet1**;**

**assign** s\_logisimBus62**[**1**]** **=** s\_logisimNet1**;**

**assign** s\_logisimBus62**[**2**]** **=** s\_logisimNet1**;**

**assign** s\_logisimBus62**[**3**]** **=** s\_logisimNet1**;**

\*\* Here all input connections are defined \*\*

**assign** s\_logisimBus106**[**5**:**0**]** **=** D\_secs**;**

**assign** s\_logisimBus110**[**5**:**0**]** **=** D\_Mins**;**

**assign** s\_logisimBus42**[**5**:**0**]** **=** D\_hours**;**

**assign** s\_logisimNet13 **=** Reset**;**

**assign** s\_logisimNet14 **=** LoadTime**;**

**assign** s\_logisimNet18 **=** AlarmEnable**;**

**assign** s\_logisimNet22 **=** LoadAlarm**;**

**assign** s\_logisimNet57 **=** AM\_PM**;**

\*\* Here all in-lined components are defined \*\*

// Ground

**assign** s\_logisimNet28 **=** 1'b0**;**

// Power

**assign** s\_logisimNet47 **=** 1'b1**;**

// Constant

**assign** s\_logisimBus15**[**3**:**0**]** **=** 4'hA**;**

// Constant

**assign** s\_logisimBus127**[**3**:**0**]** **=** 4'h6**;**

// Constant

**assign** s\_logisimBus20**[**3**:**0**]** **=** 4'hA**;**

// Constant

**assign** s\_logisimBus128**[**3**:**0**]** **=** 4'h6**;**

// Constant

**assign** s\_logisimBus23**[**3**:**0**]** **=** 4'hA**;**

// Constant

**assign** s\_logisimBus129**[**3**:**0**]** **=** 4'h2**;**

// 7-Segment Display: Status

**assign** logisimOutputBubbles**[**0**]** **=** s\_logisimBus130**[**6**];**

**assign** logisimOutputBubbles**[**1**]** **=** s\_logisimBus130**[**5**];**

**assign** logisimOutputBubbles**[**2**]** **=** s\_logisimBus130**[**4**];**

**assign** logisimOutputBubbles**[**3**]** **=** s\_logisimBus130**[**3**];**

**assign** logisimOutputBubbles**[**4**]** **=** s\_logisimBus130**[**2**];**

**assign** logisimOutputBubbles**[**5**]** **=** s\_logisimBus130**[**1**];**

**assign** logisimOutputBubbles**[**6**]** **=** s\_logisimBus130**[**0**];**

**assign** logisimOutputBubbles**[**7**]** **=** s\_logisimNet16**;**

// 7-Segment Display: MT\_O

**assign** logisimOutputBubbles**[**10**]** **=** s\_logisimNet76**;**

**assign** logisimOutputBubbles**[**11**]** **=** s\_logisimNet38**;**

**assign** logisimOutputBubbles**[**12**]** **=** s\_logisimNet96**;**

**assign** logisimOutputBubbles**[**13**]** **=** s\_logisimNet52**;**

**assign** logisimOutputBubbles**[**14**]** **=** s\_logisimNet87**;**

**assign** logisimOutputBubbles**[**15**]** **=** s\_logisimNet16**;**

**assign** logisimOutputBubbles**[**8**]** **=** s\_logisimNet24**;**

**assign** logisimOutputBubbles**[**9**]** **=** s\_logisimNet5**;**

// 7-Segment Display: SO\_O

**assign** logisimOutputBubbles**[**16**]** **=** s\_logisimNet65**;**

**assign** logisimOutputBubbles**[**17**]** **=** s\_logisimNet93**;**

**assign** logisimOutputBubbles**[**18**]** **=** s\_logisimNet131**;**

**assign** logisimOutputBubbles**[**19**]** **=** s\_logisimNet44**;**

**assign** logisimOutputBubbles**[**20**]** **=** s\_logisimNet97**;**

**assign** logisimOutputBubbles**[**21**]** **=** s\_logisimNet46**;**

**assign** logisimOutputBubbles**[**22**]** **=** s\_logisimNet77**;**

**assign** logisimOutputBubbles**[**23**]** **=** s\_logisimNet16**;**

// Constant

**assign** s\_logisimBus116**[**6**:**0**]** **=** **{**3'b000**,** 4'h0**};**

// Constant

**assign** s\_logisimBus99**[**6**:**0**]** **=** **{**3'b111**,** 4'h7**};**

// NOT Gate

**assign** s\_logisimNet82 **=** **~**s\_logisimBus109**[**1**];**

// Constant

**assign** s\_logisimBus60**[**6**:**0**]** **=** **{**3'b110**,** 4'h7**};**

// 7-Segment Display: MO\_O

**assign** logisimOutputBubbles**[**24**]** **=** s\_logisimNet50**;**

**assign** logisimOutputBubbles**[**25**]** **=** s\_logisimNet58**;**

**assign** logisimOutputBubbles**[**26**]** **=** s\_logisimNet117**;**

**assign** logisimOutputBubbles**[**27**]** **=** s\_logisimNet10**;**

**assign** logisimOutputBubbles**[**28**]** **=** s\_logisimNet9**;**

**assign** logisimOutputBubbles**[**29**]** **=** s\_logisimNet113**;**

**assign** logisimOutputBubbles**[**30**]** **=** s\_logisimNet114**;**

**assign** logisimOutputBubbles**[**31**]** **=** s\_logisimNet1**;**

// Constant

**assign** s\_logisimBus120**[**6**:**0**]** **=** **{**3'b000**,** 4'hE**};**

// 7-Segment Display: HO\_O

**assign** logisimOutputBubbles**[**32**]** **=** s\_logisimNet3**;**

**assign** logisimOutputBubbles**[**33**]** **=** s\_logisimNet108**;**

**assign** logisimOutputBubbles**[**34**]** **=** s\_logisimNet75**;**

**assign** logisimOutputBubbles**[**35**]** **=** s\_logisimNet121**;**

**assign** logisimOutputBubbles**[**36**]** **=** s\_logisimNet61**;**

**assign** logisimOutputBubbles**[**37**]** **=** s\_logisimNet40**;**

**assign** logisimOutputBubbles**[**38**]** **=** s\_logisimNet41**;**

**assign** logisimOutputBubbles**[**39**]** **=** s\_logisimNet1**;**

// 7-Segment Display: ST\_O

**assign** logisimOutputBubbles**[**40**]** **=** s\_logisimNet30**;**

**assign** logisimOutputBubbles**[**41**]** **=** s\_logisimNet31**;**

**assign** logisimOutputBubbles**[**42**]** **=** s\_logisimNet88**;**

**assign** logisimOutputBubbles**[**43**]** **=** s\_logisimNet63**;**

**assign** logisimOutputBubbles**[**44**]** **=** s\_logisimNet55**;**

**assign** logisimOutputBubbles**[**45**]** **=** s\_logisimNet67**;**

**assign** logisimOutputBubbles**[**46**]** **=** s\_logisimNet33**;**

**assign** logisimOutputBubbles**[**47**]** **=** s\_logisimNet16**;**

// 7-Segment Display: HT\_O

**assign** logisimOutputBubbles**[**48**]** **=** s\_logisimNet132**;**

**assign** logisimOutputBubbles**[**49**]** **=** s\_logisimNet95**;**

**assign** logisimOutputBubbles**[**50**]** **=** s\_logisimNet48**;**

**assign** logisimOutputBubbles**[**51**]** **=** s\_logisimNet112**;**

**assign** logisimOutputBubbles**[**52**]** **=** s\_logisimNet7**;**

**assign** logisimOutputBubbles**[**53**]** **=** s\_logisimNet8**;**

**assign** logisimOutputBubbles**[**54**]** **=** s\_logisimNet72**;**

**assign** logisimOutputBubbles**[**55**]** **=** s\_logisimNet16**;**

// Constant

**assign** s\_logisimBus133**[**3**:**0**]** **=** 4'h2**;**

// Constant

**assign** s\_logisimBus49**[**3**:**0**]** **=** 4'h1**;**

// Ground

**assign** s\_logisimNet16 **=** 1'b0**;**

\*\* Here all normal components are defined \*\*

OR\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_1 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet14**),**

**.**result**(**s\_logisimNet135**));**

OR\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_2 **(.**input1**(**s\_logisimNet21**),**

**.**input2**(**s\_logisimNet11**),**

**.**result**(**s\_logisimNet104**));**

Comparator **#(.**nrOfBits**(**4**),**

**.**twosComplement**(**1**))**

ARITH\_3 **(.**aEqualsB**(**s\_logisimNet11**),**

**.**aGreaterThanB**(),**

**.**aLessThanB**(),**

**.**dataA**(**s\_logisimBus4**[**3**:**0**]),**

**.**dataB**(**s\_logisimBus15**[**3**:**0**]));**

LogisimCounter **#(.**invertClock**(**0**),**

**.**maxVal**(**4'hF**),**

**.**mode**(**0**),**

**.**width**(**4**))**

MEMORY\_4 **(.**clear**(**s\_logisimNet104**),**

**.**clock**(**s\_logisimNet135**),**

**.**compareOut**(),**

**.**countValue**(**s\_logisimBus4**[**3**:**0**]),**

**.**enable**(**s\_logisimNet47**),**

**.**load**(**s\_logisimNet14**),**

**.**loadData**(**s\_logisimBus32**[**3**:**0**]),**

**.**tick**(**1'b1**),**

**.**upNotDown**(**s\_logisimNet47**));**

LogisimCounter **#(.**invertClock**(**0**),**

**.**maxVal**(**4'hF**),**

**.**mode**(**0**),**

**.**width**(**4**))**

MEMORY\_5 **(.**clear**(**s\_logisimNet101**),**

**.**clock**(**s\_logisimNet125**),**

**.**compareOut**(),**

**.**countValue**(**s\_logisimBus26**[**3**:**0**]),**

**.**enable**(**s\_logisimNet47**),**

**.**load**(**s\_logisimNet14**),**

**.**loadData**(**s\_logisimBus51**[**3**:**0**]),**

**.**tick**(**1'b1**),**

**.**upNotDown**(**s\_logisimNet47**));**

OR\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_6 **(.**input1**(**s\_logisimNet11**),**

**.**input2**(**s\_logisimNet14**),**

**.**result**(**s\_logisimNet125**));**

Comparator **#(.**nrOfBits**(**4**),**

**.**twosComplement**(**1**))**

ARITH\_7 **(.**aEqualsB**(**s\_logisimNet69**),**

**.**aGreaterThanB**(),**

**.**aLessThanB**(),**

**.**dataA**(**s\_logisimBus26**[**3**:**0**]),**

**.**dataB**(**s\_logisimBus127**[**3**:**0**]));**

OR\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_8 **(.**input1**(**s\_logisimNet21**),**

**.**input2**(**s\_logisimNet69**),**

**.**result**(**s\_logisimNet101**));**

OR\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_9 **(.**input1**(**s\_logisimNet21**),**

**.**input2**(**s\_logisimNet74**),**

**.**result**(**s\_logisimNet100**));**

Comparator **#(.**nrOfBits**(**4**),**

**.**twosComplement**(**1**))**

ARITH\_10 **(.**aEqualsB**(**s\_logisimNet12**),**

**.**aGreaterThanB**(),**

**.**aLessThanB**(),**

**.**dataA**(**s\_logisimBus34**[**3**:**0**]),**

**.**dataB**(**s\_logisimBus20**[**3**:**0**]));**

OR\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_11 **(.**input1**(**s\_logisimNet69**),**

**.**input2**(**s\_logisimNet14**),**

**.**result**(**s\_logisimNet134**));**

LogisimCounter **#(.**invertClock**(**0**),**

**.**maxVal**(**4'hF**),**

**.**mode**(**0**),**

**.**width**(**4**))**

MEMORY\_12 **(.**clear**(**s\_logisimNet100**),**

**.**clock**(**s\_logisimNet124**),**

**.**compareOut**(),**

**.**countValue**(**s\_logisimBus27**[**3**:**0**]),**

**.**enable**(**s\_logisimNet47**),**

**.**load**(**s\_logisimNet14**),**

**.**loadData**(**s\_logisimBus54**[**3**:**0**]),**

**.**tick**(**1'b1**),**

**.**upNotDown**(**s\_logisimNet47**));**

LogisimCounter **#(.**invertClock**(**0**),**

**.**maxVal**(**4'hF**),**

**.**mode**(**0**),**

**.**width**(**4**))**

MEMORY\_13 **(.**clear**(**s\_logisimNet103**),**

**.**clock**(**s\_logisimNet134**),**

**.**compareOut**(),**

**.**countValue**(**s\_logisimBus34**[**3**:**0**]),**

**.**enable**(**s\_logisimNet47**),**

**.**load**(**s\_logisimNet14**),**

**.**loadData**(**s\_logisimBus68**[**3**:**0**]),**

**.**tick**(**1'b1**),**

**.**upNotDown**(**s\_logisimNet47**));**

OR\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_14 **(.**input1**(**s\_logisimNet12**),**

**.**input2**(**s\_logisimNet14**),**

**.**result**(**s\_logisimNet124**));**

Comparator **#(.**nrOfBits**(**4**),**

**.**twosComplement**(**1**))**

ARITH\_15 **(.**aEqualsB**(**s\_logisimNet74**),**

**.**aGreaterThanB**(),**

**.**aLessThanB**(),**

**.**dataA**(**s\_logisimBus27**[**3**:**0**]),**

**.**dataB**(**s\_logisimBus128**[**3**:**0**]));**

OR\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_16 **(.**input1**(**s\_logisimNet21**),**

**.**input2**(**s\_logisimNet12**),**

**.**result**(**s\_logisimNet103**));**

Comparator **#(.**nrOfBits**(**4**),**

**.**twosComplement**(**1**))**

ARITH\_17 **(.**aEqualsB**(**s\_logisimNet71**),**

**.**aGreaterThanB**(),**

**.**aLessThanB**(),**

**.**dataA**(**s\_logisimBus25**[**3**:**0**]),**

**.**dataB**(**s\_logisimBus129**[**3**:**0**]));**

OR\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_18 **(.**input1**(**s\_logisimNet73**),**

**.**input2**(**s\_logisimNet14**),**

**.**result**(**s\_logisimNet126**));**

OR\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_19 **(.**input1**(**s\_logisimNet21**),**

**.**input2**(**s\_logisimNet73**),**

**.**result**(**s\_logisimNet102**));**

LogisimCounter **#(.**invertClock**(**0**),**

**.**maxVal**(**4'hF**),**

**.**mode**(**0**),**

**.**width**(**4**))**

MEMORY\_20 **(.**clear**(**s\_logisimNet105**),**

**.**clock**(**s\_logisimNet126**),**

**.**compareOut**(),**

**.**countValue**(**s\_logisimBus25**[**3**:**0**]),**

**.**enable**(**s\_logisimNet47**),**

**.**load**(**s\_logisimNet14**),**

**.**loadData**(**s\_logisimBus89**[**3**:**0**]),**

**.**tick**(**1'b1**),**

**.**upNotDown**(**s\_logisimNet47**));**

LogisimCounter **#(.**invertClock**(**0**),**

**.**maxVal**(**4'hF**),**

**.**mode**(**0**),**

**.**width**(**4**))**

MEMORY\_21 **(.**clear**(**s\_logisimNet102**),**

**.**clock**(**s\_logisimNet136**),**

**.**compareOut**(),**

**.**countValue**(**s\_logisimBus6**[**3**:**0**]),**

**.**enable**(**s\_logisimNet47**),**

**.**load**(**s\_logisimNet14**),**

**.**loadData**(**s\_logisimBus36**[**3**:**0**]),**

**.**tick**(**1'b1**),**

**.**upNotDown**(**s\_logisimNet47**));**

OR\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_22 **(.**input1**(**s\_logisimNet21**),**

**.**input2**(**s\_logisimNet71**),**

**.**result**(**s\_logisimNet105**));**

OR\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_23 **(.**input1**(**s\_logisimNet74**),**

**.**input2**(**s\_logisimNet14**),**

**.**result**(**s\_logisimNet136**));**

Comparator **#(.**nrOfBits**(**4**),**

**.**twosComplement**(**1**))**

ARITH\_24 **(.**aEqualsB**(**s\_logisimNet73**),**

**.**aGreaterThanB**(),**

**.**aLessThanB**(),**

**.**dataA**(**s\_logisimBus6**[**3**:**0**]),**

**.**dataB**(**s\_logisimBus23**[**3**:**0**]));**

REGISTER\_FLIP\_FLOP **#(.**invertClock**(**0**),**

**.**nrOfBits**(**2**))**

MEMORY\_25 **(.**clock**(**logisimClockTree0**[**4**]),**

**.**clockEnable**(**s\_logisimNet47**),**

**.**d**(**s\_logisimBus109**[**1**:**0**]),**

**.**q**(**s\_logisimBus56**[**1**:**0**]),**

**.**reset**(**s\_logisimNet13**),**

**.**tick**(**logisimClockTree0**[**2**]));**

D\_FLIPFLOP **#(.**invertClockEnable**(**0**))**

MEMORY\_26 **(.**clock**(**s\_logisimNet64**),**

**.**d**(**s\_logisimNet82**),**

**.**preset**(**1'b0**),**

**.**q**(**s\_logisimBus109**[**1**]),**

**.**qBar**(**s\_logisimBus109**[**0**]),**

**.**reset**(**s\_logisimNet13**),**

**.**tick**(**1'b1**));**

Multiplexer\_bus\_4 **#(.**nrOfBits**(**7**))**

PLEXERS\_27 **(.**enable**(**1'b1**),**

**.**muxIn\_0**(**s\_logisimBus116**[**6**:**0**]),**

**.**muxIn\_1**(**s\_logisimBus99**[**6**:**0**]),**

**.**muxIn\_2**(**s\_logisimBus60**[**6**:**0**]),**

**.**muxIn\_3**(**s\_logisimBus120**[**6**:**0**]),**

**.**muxOut**(**s\_logisimBus130**[**6**:**0**]),**

**.**sel**(**s\_logisimBus56**[**1**:**0**]));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_28 **(.**input1**(**s\_logisimNet123**),**

**.**input2**(**s\_logisimNet91**),**

**.**result**(**s\_logisimNet90**));**

Comparator **#(.**nrOfBits**(**4**),**

**.**twosComplement**(**1**))**

ARITH\_29 **(.**aEqualsB**(**s\_logisimNet91**),**

**.**aGreaterThanB**(),**

**.**aLessThanB**(),**

**.**dataA**(**s\_logisimBus25**[**3**:**0**]),**

**.**dataB**(**s\_logisimBus49**[**3**:**0**]));**

Comparator **#(.**nrOfBits**(**4**),**

**.**twosComplement**(**1**))**

ARITH\_30 **(.**aEqualsB**(**s\_logisimNet123**),**

**.**aGreaterThanB**(),**

**.**aLessThanB**(),**

**.**dataA**(**s\_logisimBus133**[**3**:**0**]),**

**.**dataB**(**s\_logisimBus6**[**3**:**0**]));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_31 **(.**input1**(**s\_logisimNet57**),**

**.**input2**(**s\_logisimNet14**),**

**.**result**(**s\_logisimNet115**));**

OR\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_32 **(.**input1**(**s\_logisimNet90**),**

**.**input2**(**s\_logisimNet13**),**

**.**result**(**s\_logisimNet21**));**

OR\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_33 **(.**input1**(**s\_logisimNet115**),**

**.**input2**(**s\_logisimNet90**),**

**.**result**(**s\_logisimNet64**));**

Multiplexer\_bus\_4 **#(.**nrOfBits**(**4**))**

PLEXERS\_34 **(.**enable**(**1'b1**),**

**.**muxIn\_0**(**s\_logisimBus6**[**3**:**0**]),**

**.**muxIn\_1**(**s\_logisimBus36**[**3**:**0**]),**

**.**muxIn\_2**(**s\_logisimBus59**[**3**:**0**]),**

**.**muxIn\_3**(**s\_logisimBus62**[**3**:**0**]),**

**.**muxOut**(**s\_logisimBus111**[**3**:**0**]),**

**.**sel**(**s\_logisimBus17**[**1**:**0**]));**

Multiplexer\_bus\_4 **#(.**nrOfBits**(**4**))**

PLEXERS\_35 **(.**enable**(**1'b1**),**

**.**muxIn\_0**(**s\_logisimBus25**[**3**:**0**]),**

**.**muxIn\_1**(**s\_logisimBus89**[**3**:**0**]),**

**.**muxIn\_2**(**s\_logisimBus85**[**3**:**0**]),**

**.**muxIn\_3**(**s\_logisimBus62**[**3**:**0**]),**

**.**muxOut**(**s\_logisimBus92**[**3**:**0**]),**

**.**sel**(**s\_logisimBus17**[**1**:**0**]));**

Multiplexer\_bus\_4 **#(.**nrOfBits**(**4**))**

PLEXERS\_36 **(.**enable**(**1'b1**),**

**.**muxIn\_0**(**s\_logisimBus34**[**3**:**0**]),**

**.**muxIn\_1**(**s\_logisimBus68**[**3**:**0**]),**

**.**muxIn\_2**(**s\_logisimBus2**[**3**:**0**]),**

**.**muxIn\_3**(**s\_logisimBus62**[**3**:**0**]),**

**.**muxOut**(**s\_logisimBus43**[**3**:**0**]),**

**.**sel**(**s\_logisimBus17**[**1**:**0**]));**

Multiplexer\_bus\_4 **#(.**nrOfBits**(**4**))**

PLEXERS\_37 **(.**enable**(**1'b1**),**

**.**muxIn\_0**(**s\_logisimBus26**[**3**:**0**]),**

**.**muxIn\_1**(**s\_logisimBus51**[**3**:**0**]),**

**.**muxIn\_2**(**s\_logisimBus80**[**3**:**0**]),**

**.**muxIn\_3**(**s\_logisimBus62**[**3**:**0**]),**

**.**muxOut**(**s\_logisimBus37**[**3**:**0**]),**

**.**sel**(**s\_logisimBus17**[**1**:**0**]));**

Multiplexer\_bus\_4 **#(.**nrOfBits**(**4**))**

PLEXERS\_38 **(.**enable**(**1'b1**),**

**.**muxIn\_0**(**s\_logisimBus27**[**3**:**0**]),**

**.**muxIn\_1**(**s\_logisimBus54**[**3**:**0**]),**

**.**muxIn\_2**(**s\_logisimBus79**[**3**:**0**]),**

**.**muxIn\_3**(**s\_logisimBus62**[**3**:**0**]),**

**.**muxOut**(**s\_logisimBus19**[**3**:**0**]),**

**.**sel**(**s\_logisimBus17**[**1**:**0**]));**

Multiplexer\_bus\_4 **#(.**nrOfBits**(**4**))**

PLEXERS\_39 **(.**enable**(**1'b1**),**

**.**muxIn\_0**(**s\_logisimBus4**[**3**:**0**]),**

**.**muxIn\_1**(**s\_logisimBus32**[**3**:**0**]),**

**.**muxIn\_2**(**s\_logisimBus0**[**3**:**0**]),**

**.**muxIn\_3**(**s\_logisimBus62**[**3**:**0**]),**

**.**muxOut**(**s\_logisimBus86**[**3**:**0**]),**

**.**sel**(**s\_logisimBus17**[**1**:**0**]));**

REGISTER\_FLIP\_FLOP **#(.**invertClock**(**0**),**

**.**nrOfBits**(**4**))**

MEMORY\_40 **(.**clock**(**logisimClockTree0**[**4**]),**

**.**clockEnable**(**s\_logisimNet22**),**

**.**d**(**s\_logisimBus54**[**3**:**0**]),**

**.**q**(**s\_logisimBus79**[**3**:**0**]),**

**.**reset**(**1'b0**),**

**.**tick**(**logisimClockTree0**[**2**]));**

REGISTER\_FLIP\_FLOP **#(.**invertClock**(**0**),**

**.**nrOfBits**(**4**))**

MEMORY\_41 **(.**clock**(**logisimClockTree0**[**4**]),**

**.**clockEnable**(**s\_logisimNet22**),**

**.**d**(**s\_logisimBus68**[**3**:**0**]),**

**.**q**(**s\_logisimBus2**[**3**:**0**]),**

**.**reset**(**1'b0**),**

**.**tick**(**logisimClockTree0**[**2**]));**

REGISTER\_FLIP\_FLOP **#(.**invertClock**(**0**),**

**.**nrOfBits**(**4**))**

MEMORY\_42 **(.**clock**(**logisimClockTree0**[**4**]),**

**.**clockEnable**(**s\_logisimNet22**),**

**.**d**(**s\_logisimBus36**[**3**:**0**]),**

**.**q**(**s\_logisimBus59**[**3**:**0**]),**

**.**reset**(**1'b0**),**

**.**tick**(**logisimClockTree0**[**2**]));**

REGISTER\_FLIP\_FLOP **#(.**invertClock**(**0**),**

**.**nrOfBits**(**4**))**

MEMORY\_43 **(.**clock**(**logisimClockTree0**[**4**]),**

**.**clockEnable**(**s\_logisimNet22**),**

**.**d**(**s\_logisimBus89**[**3**:**0**]),**

**.**q**(**s\_logisimBus85**[**3**:**0**]),**

**.**reset**(**1'b0**),**

**.**tick**(**logisimClockTree0**[**2**]));**

priority\_encoder PLEXERS\_44 **(.**A0**(**s\_logisimBus17**[**0**]),**

**.**A1**(**s\_logisimBus17**[**1**]),**

**.**Y0**(**s\_logisimNet47**),.**Y1**(**s\_logisimNet14**),.**Y2**(**s\_logisimNet22**),.**Y3**(**s\_logisimNet29**));**

REGISTER\_FLIP\_FLOP **#(.**invertClock**(**0**),**

**.**nrOfBits**(**4**))**

MEMORY\_45 **(.**clock**(**logisimClockTree0**[**4**]),**

**.**clockEnable**(**s\_logisimNet22**),**

**.**d**(**s\_logisimBus51**[**3**:**0**]),**

**.**q**(**s\_logisimBus80**[**3**:**0**]),**

**.**reset**(**1'b0**),**

**.**tick**(**logisimClockTree0**[**2**]));**

REGISTER\_FLIP\_FLOP **#(.**invertClock**(**0**),**

**.**nrOfBits**(**4**))**

MEMORY\_46 **(.**clock**(**logisimClockTree0**[**4**]),**

**.**clockEnable**(**s\_logisimNet22**),**

**.**d**(**s\_logisimBus32**[**3**:**0**]),**

**.**q**(**s\_logisimBus0**[**3**:**0**]),**

**.**reset**(**1'b0**),**

**.**tick**(**logisimClockTree0**[**2**]));**

Comparator **#(.**nrOfBits**(**4**),**

**.**twosComplement**(**1**))**

ARITH\_47 **(.**aEqualsB**(**s\_logisimNet45**),**

**.**aGreaterThanB**(),**

**.**aLessThanB**(),**

**.**dataA**(**s\_logisimBus25**[**3**:**0**]),**

**.**dataB**(**s\_logisimBus85**[**3**:**0**]));**

Comparator **#(.**nrOfBits**(**4**),**

**.**twosComplement**(**1**))**

ARITH\_48 **(.**aEqualsB**(**s\_logisimNet122**),**

**.**aGreaterThanB**(),**

**.**aLessThanB**(),**

**.**dataA**(**s\_logisimBus6**[**3**:**0**]),**

**.**dataB**(**s\_logisimBus59**[**3**:**0**]));**

Comparator **#(.**nrOfBits**(**4**),**

**.**twosComplement**(**1**))**

ARITH\_49 **(.**aEqualsB**(**s\_logisimNet118**),**

**.**aGreaterThanB**(),**

**.**aLessThanB**(),**

**.**dataA**(**s\_logisimBus27**[**3**:**0**]),**

**.**dataB**(**s\_logisimBus79**[**3**:**0**]));**

Comparator **#(.**nrOfBits**(**4**),**

**.**twosComplement**(**1**))**

ARITH\_50 **(.**aEqualsB**(**s\_logisimNet39**),**

**.**aGreaterThanB**(),**

**.**aLessThanB**(),**

**.**dataA**(**s\_logisimBus34**[**3**:**0**]),**

**.**dataB**(**s\_logisimBus2**[**3**:**0**]));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_51 **(.**input1**(**s\_logisimNet39**),**

**.**input2**(**s\_logisimNet118**),**

**.**input3**(**s\_logisimNet122**),**

**.**input4**(**s\_logisimNet45**),**

**.**result**(**s\_logisimNet81**));**

REGISTER\_FLIP\_FLOP **#(.**invertClock**(**0**),**

**.**nrOfBits**(**1**))**

MEMORY\_52 **(.**clock**(**logisimClockTree0**[**4**]),**

**.**clockEnable**(**s\_logisimNet18**),**

**.**d**(**s\_logisimNet81**),**

**.**q**(**s\_logisimNet29**),**

**.**reset**(**s\_logisimNet35**),**

**.**tick**(**logisimClockTree0**[**2**]));**

OR\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_53 **(.**input1**(**s\_logisimNet98**),**

**.**input2**(**s\_logisimNet13**),**

**.**result**(**s\_logisimNet35**));**

REGISTER\_FLIP\_FLOP **#(.**invertClock**(**0**),**

**.**nrOfBits**(**1**))**

MEMORY\_54 **(.**clock**(**logisimClockTree0**[**4**]),**

**.**clockEnable**(**s\_logisimNet18**),**

**.**d**(**s\_logisimNet11**),**

**.**q**(**s\_logisimNet98**),**

**.**reset**(**s\_logisimNet12**),**

**.**tick**(**logisimClockTree0**[**2**]));**

\*\* Here all sub-circuits are defined \*\*

Bin\_to\_BCD Sec\_c **(.**D0**(**s\_logisimBus106**[**5**]),**

**.**D1**(**s\_logisimBus106**[**4**]),**

**.**D2**(**s\_logisimBus106**[**3**]),**

**.**D3**(**s\_logisimBus106**[**2**]),**

**.**D4**(**s\_logisimBus106**[**1**]),**

**.**D5**(**s\_logisimBus106**[**0**]),**

**.**O0**(**s\_logisimBus51**[**3**]),**

**.**O1**(**s\_logisimBus51**[**2**]),**

**.**O2**(**s\_logisimBus51**[**1**]),**

**.**O3**(**s\_logisimBus51**[**0**]),**

**.**T0**(**s\_logisimBus32**[**3**]),**

**.**T1**(**s\_logisimBus32**[**2**]),**

**.**T2**(**s\_logisimBus32**[**1**]),**

**.**T3**(**s\_logisimBus32**[**0**]),**

**.**logisimClockTree0**(**logisimClockTree0**));**

Bin\_to\_BCD Min\_c **(.**D0**(**s\_logisimBus110**[**5**]),**

**.**D1**(**s\_logisimBus110**[**4**]),**

**.**D2**(**s\_logisimBus110**[**3**]),**

**.**D3**(**s\_logisimBus110**[**2**]),**

**.**D4**(**s\_logisimBus110**[**1**]),**

**.**D5**(**s\_logisimBus110**[**0**]),**

**.**O0**(**s\_logisimBus54**[**3**]),**

**.**O1**(**s\_logisimBus54**[**2**]),**

**.**O2**(**s\_logisimBus54**[**1**]),**

**.**O3**(**s\_logisimBus54**[**0**]),**

**.**T0**(**s\_logisimBus68**[**3**]),**

**.**T1**(**s\_logisimBus68**[**2**]),**

**.**T2**(**s\_logisimBus68**[**1**]),**

**.**T3**(**s\_logisimBus68**[**0**]),**

**.**logisimClockTree0**(**logisimClockTree0**));**

Bin\_to\_BCD Hour\_c **(.**D0**(**s\_logisimBus42**[**5**]),**

**.**D1**(**s\_logisimBus42**[**4**]),**

**.**D2**(**s\_logisimBus42**[**3**]),**

**.**D3**(**s\_logisimBus42**[**2**]),**

**.**D4**(**s\_logisimBus42**[**1**]),**

**.**D5**(**s\_logisimBus42**[**0**]),**

**.**O0**(**s\_logisimBus89**[**3**]),**

**.**O1**(**s\_logisimBus89**[**2**]),**

**.**O2**(**s\_logisimBus89**[**1**]),**

**.**O3**(**s\_logisimBus89**[**0**]),**

**.**T0**(**s\_logisimBus36**[**3**]),**

**.**T1**(**s\_logisimBus36**[**2**]),**

**.**T2**(**s\_logisimBus36**[**1**]),**

**.**T3**(**s\_logisimBus36**[**0**]),**

**.**logisimClockTree0**(**logisimClockTree0**));**

BCD\_to\_7seg Sec\_seg **(.**A**(**s\_logisimNet30**),**

**.**B**(**s\_logisimNet31**),**

**.**C**(**s\_logisimNet88**),**

**.**D**(**s\_logisimNet63**),**

**.**D0**(**s\_logisimBus37**[**0**]),**

**.**D1**(**s\_logisimBus37**[**1**]),**

**.**D2**(**s\_logisimBus37**[**2**]),**

**.**D3**(**s\_logisimBus37**[**3**]),**

**.**E**(**s\_logisimNet55**),**

**.**F**(**s\_logisimNet67**),**

**.**G**(**s\_logisimNet33**),**

**.**logisimClockTree0**(**logisimClockTree0**));**

BCD\_to\_7seg Hour\_seg2 **(.**A**(**s\_logisimNet3**),**

**.**B**(**s\_logisimNet108**),**

**.**C**(**s\_logisimNet75**),**

**.**D**(**s\_logisimNet121**),**

**.**D0**(**s\_logisimBus111**[**0**]),**

**.**D1**(**s\_logisimBus111**[**1**]),**

**.**D2**(**s\_logisimBus111**[**2**]),**

**.**D3**(**s\_logisimBus111**[**3**]),**

**.**E**(**s\_logisimNet61**),**

**.**F**(**s\_logisimNet40**),**

**.**G**(**s\_logisimNet41**),**

**.**logisimClockTree0**(**logisimClockTree0**));**

BCD\_to\_7seg Hour\_seg **(.**A**(**s\_logisimNet132**),**

**.**B**(**s\_logisimNet95**),**

**.**C**(**s\_logisimNet48**),**

**.**D**(**s\_logisimNet112**),**

**.**D0**(**s\_logisimBus92**[**0**]),**

**.**D1**(**s\_logisimBus92**[**1**]),**

**.**D2**(**s\_logisimBus92**[**2**]),**

**.**D3**(**s\_logisimBus92**[**3**]),**

**.**E**(**s\_logisimNet7**),**

**.**F**(**s\_logisimNet8**),**

**.**G**(**s\_logisimNet72**),**

**.**logisimClockTree0**(**logisimClockTree0**));**

BCD\_to\_7seg Min\_seg2 **(.**A**(**s\_logisimNet50**),**

**.**B**(**s\_logisimNet58**),**

**.**C**(**s\_logisimNet117**),**

**.**D**(**s\_logisimNet10**),**

**.**D0**(**s\_logisimBus43**[**0**]),**

**.**D1**(**s\_logisimBus43**[**1**]),**

**.**D2**(**s\_logisimBus43**[**2**]),**

**.**D3**(**s\_logisimBus43**[**3**]),**

**.**E**(**s\_logisimNet9**),**

**.**F**(**s\_logisimNet113**),**

**.**G**(**s\_logisimNet114**),**

**.**logisimClockTree0**(**logisimClockTree0**));**

BCD\_to\_7seg Min\_seg **(.**A**(**s\_logisimNet24**),**

**.**B**(**s\_logisimNet5**),**

**.**C**(**s\_logisimNet76**),**

**.**D**(**s\_logisimNet38**),**

**.**D0**(**s\_logisimBus19**[**0**]),**

**.**D1**(**s\_logisimBus19**[**1**]),**

**.**D2**(**s\_logisimBus19**[**2**]),**

**.**D3**(**s\_logisimBus19**[**3**]),**

**.**E**(**s\_logisimNet96**),**

**.**F**(**s\_logisimNet52**),**

**.**G**(**s\_logisimNet87**),**

**.**logisimClockTree0**(**logisimClockTree0**));**

BCD\_to\_7seg Sec\_seg2 **(.**A**(**s\_logisimNet65**),**

**.**B**(**s\_logisimNet93**),**

**.**C**(**s\_logisimNet131**),**

**.**D**(**s\_logisimNet44**),**

**.**D0**(**s\_logisimBus86**[**0**]),**

**.**D1**(**s\_logisimBus86**[**1**]),**

**.**D2**(**s\_logisimBus86**[**2**]),**

**.**D3**(**s\_logisimBus86**[**3**]),**

**.**E**(**s\_logisimNet97**),**

**.**F**(**s\_logisimNet46**),**

**.**G**(**s\_logisimNet77**),**

**.**logisimClockTree0**(**logisimClockTree0**));**

**endmodule**

* TopLevelShell.v

**module** logisimTopLevelShell**(** AM\_PM\_0**,**

AlarmEnable\_0**,**

D\_Mins\_0**,**

D\_Mins\_1**,**

D\_Mins\_2**,**

D\_Mins\_3**,**

D\_Mins\_4**,**

D\_Mins\_5**,**

D\_hours\_0**,**

D\_hours\_1**,**

D\_hours\_2**,**

D\_hours\_3**,**

D\_hours\_4**,**

D\_hours\_5**,**

D\_secs\_0**,**

D\_secs\_1**,**

D\_secs\_2**,**

D\_secs\_3**,**

D\_secs\_4**,**

D\_secs\_5**,**

HO\_O\_Segment\_A**,**

HO\_O\_Segment\_B**,**

HO\_O\_Segment\_C**,**

HO\_O\_Segment\_D**,**

HO\_O\_Segment\_E**,**

HO\_O\_Segment\_F**,**

HO\_O\_Segment\_G**,**

HT\_O\_Segment\_A**,**

HT\_O\_Segment\_B**,**

HT\_O\_Segment\_C**,**

HT\_O\_Segment\_D**,**

HT\_O\_Segment\_E**,**

HT\_O\_Segment\_F**,**

HT\_O\_Segment\_G**,**

LoadAlarm\_0**,**

LoadTime\_0**,**

MO\_O\_Segment\_A**,**

MO\_O\_Segment\_B**,**

MO\_O\_Segment\_C**,**

MO\_O\_Segment\_D**,**

MO\_O\_Segment\_E**,**

MO\_O\_Segment\_F**,**

MO\_O\_Segment\_G**,**

MT\_O\_Segment\_A**,**

MT\_O\_Segment\_B**,**

MT\_O\_Segment\_C**,**

MT\_O\_Segment\_D**,**

fpgaGlobalClock**,**

n\_Reset\_0 **);**

\*\* The inputs are defined here \*\*

**input** AM\_PM\_0**;**

**input** AlarmEnable\_0**;**

**input** D\_Mins\_0**;**

**input** D\_Mins\_1**;**

**input** D\_Mins\_2**;**

**input** D\_Mins\_3**;**

**input** D\_Mins\_4**;**

**input** D\_Mins\_5**;**

**input** D\_hours\_0**;**

**input** D\_hours\_1**;**

**input** D\_hours\_2**;**

**input** D\_hours\_3**;**

**input** D\_hours\_4**;**

**input** D\_hours\_5**;**

**input** D\_secs\_0**;**

**input** D\_secs\_1**;**

**input** D\_secs\_2**;**

**input** D\_secs\_3**;**

**input** D\_secs\_4**;**

**input** D\_secs\_5**;**

**input** LoadAlarm\_0**;**

**input** LoadTime\_0**;**

**input** fpgaGlobalClock**;**

**input** n\_Reset\_0**;**

\*\* The outputs are defined here \*\*

**output** HO\_O\_Segment\_A**;**

**output** HO\_O\_Segment\_B**;**

**output** HO\_O\_Segment\_C**;**

**output** HO\_O\_Segment\_D**;**

**output** HO\_O\_Segment\_E**;**

**output** HO\_O\_Segment\_F**;**

**output** HO\_O\_Segment\_G**;**

**output** HT\_O\_Segment\_A**;**

**output** HT\_O\_Segment\_B**;**

**output** HT\_O\_Segment\_C**;**

**output** HT\_O\_Segment\_D**;**

**output** HT\_O\_Segment\_E**;**

**output** HT\_O\_Segment\_F**;**

**output** HT\_O\_Segment\_G**;**

**output** MO\_O\_Segment\_A**;**

**output** MO\_O\_Segment\_B**;**

**output** MO\_O\_Segment\_C**;**

**output** MO\_O\_Segment\_D**;**

**output** MO\_O\_Segment\_E**;**

**output** MO\_O\_Segment\_F**;**

**output** MO\_O\_Segment\_G**;**

**output** MT\_O\_Segment\_A**;**

**output** MT\_O\_Segment\_B**;**

**output** MT\_O\_Segment\_C**;**

**output** MT\_O\_Segment\_D**;**

\*\* The wires are defined here \*\*

**wire** s\_AM\_PM**;**

**wire** s\_AlarmEnable**;**

**wire** **[**5**:**0**]** s\_D\_Mins**;**

**wire** **[**5**:**0**]** s\_D\_hours**;**

**wire** **[**5**:**0**]** s\_D\_secs**;**

**wire** s\_LoadAlarm**;**

**wire** s\_LoadTime**;**

**wire** s\_Reset**;**

**wire** s\_fpgaTick**;**

**wire** **[**4**:**0**]** s\_logisimClockTree0**;**

**wire** **[**55**:**0**]** s\_logisimOutputBubbles**;**

\*\* The module functionality is described here \*\*

\*\* All signal adaptations are performed here \*\*

**assign** HO\_O\_Segment\_A **=** s\_logisimOutputBubbles**[**32**];**

**assign** HO\_O\_Segment\_B **=** s\_logisimOutputBubbles**[**33**];**

**assign** HO\_O\_Segment\_C **=** s\_logisimOutputBubbles**[**34**];**

**assign** HO\_O\_Segment\_D **=** s\_logisimOutputBubbles**[**35**];**

**assign** HO\_O\_Segment\_E **=** s\_logisimOutputBubbles**[**36**];**

**assign** HO\_O\_Segment\_F **=** s\_logisimOutputBubbles**[**37**];**

**assign** HO\_O\_Segment\_G **=** s\_logisimOutputBubbles**[**38**];**

**assign** HT\_O\_Segment\_A **=** s\_logisimOutputBubbles**[**48**];**

**assign** HT\_O\_Segment\_B **=** s\_logisimOutputBubbles**[**49**];**

**assign** HT\_O\_Segment\_C **=** s\_logisimOutputBubbles**[**50**];**

**assign** HT\_O\_Segment\_D **=** s\_logisimOutputBubbles**[**51**];**

**assign** HT\_O\_Segment\_E **=** s\_logisimOutputBubbles**[**52**];**

**assign** HT\_O\_Segment\_F **=** s\_logisimOutputBubbles**[**53**];**

**assign** HT\_O\_Segment\_G **=** s\_logisimOutputBubbles**[**54**];**

**assign** MO\_O\_Segment\_A **=** s\_logisimOutputBubbles**[**24**];**

**assign** MO\_O\_Segment\_B **=** s\_logisimOutputBubbles**[**25**];**

**assign** MO\_O\_Segment\_C **=** s\_logisimOutputBubbles**[**26**];**

**assign** MO\_O\_Segment\_D **=** s\_logisimOutputBubbles**[**27**];**

**assign** MO\_O\_Segment\_E **=** s\_logisimOutputBubbles**[**28**];**

**assign** MO\_O\_Segment\_F **=** s\_logisimOutputBubbles**[**29**];**

**assign** MO\_O\_Segment\_G **=** s\_logisimOutputBubbles**[**30**];**

**assign** MT\_O\_Segment\_A **=** s\_logisimOutputBubbles**[**8**];**

**assign** MT\_O\_Segment\_B **=** s\_logisimOutputBubbles**[**9**];**

**assign** MT\_O\_Segment\_C **=** s\_logisimOutputBubbles**[**10**];**

**assign** MT\_O\_Segment\_D **=** s\_logisimOutputBubbles**[**11**];**

**assign** s\_AM\_PM **=** AM\_PM\_0**;**

**assign** s\_AlarmEnable **=** AlarmEnable\_0**;**

**assign** s\_D\_Mins**[**0**]** **=** D\_Mins\_0**;**

**assign** s\_D\_Mins**[**1**]** **=** D\_Mins\_1**;**

**assign** s\_D\_Mins**[**2**]** **=** D\_Mins\_2**;**

**assign** s\_D\_Mins**[**3**]** **=** D\_Mins\_3**;**

**assign** s\_D\_Mins**[**4**]** **=** D\_Mins\_4**;**

**assign** s\_D\_Mins**[**5**]** **=** D\_Mins\_5**;**

**assign** s\_D\_hours**[**0**]** **=** D\_hours\_0**;**

**assign** s\_D\_hours**[**1**]** **=** D\_hours\_1**;**

**assign** s\_D\_hours**[**2**]** **=** D\_hours\_2**;**

**assign** s\_D\_hours**[**3**]** **=** D\_hours\_3**;**

**assign** s\_D\_hours**[**4**]** **=** D\_hours\_4**;**

**assign** s\_D\_hours**[**5**]** **=** D\_hours\_5**;**

**assign** s\_D\_secs**[**0**]** **=** D\_secs\_0**;**

**assign** s\_D\_secs**[**1**]** **=** D\_secs\_1**;**

**assign** s\_D\_secs**[**2**]** **=** D\_secs\_2**;**

**assign** s\_D\_secs**[**3**]** **=** D\_secs\_3**;**

**assign** s\_D\_secs**[**4**]** **=** D\_secs\_4**;**

**assign** s\_D\_secs**[**5**]** **=** D\_secs\_5**;**

**assign** s\_LoadAlarm **=** LoadAlarm\_0**;**

**assign** s\_LoadTime **=** LoadTime\_0**;**

**assign** s\_Reset **=** **~**n\_Reset\_0**;**

\*\* The clock tree components are defined here \*\*

logisimTickGenerator **#(.**nrOfBits**(**20**),**

**.**reloadValue**(**1000000**))**

BASE\_0 **(.**FPGAClock**(**fpgaGlobalClock**),**

**.**FPGATick**(**s\_fpgaTick**));**

LogisimClockComponent **#(.**highTicks**(**1**),**

**.**lowTicks**(**1**),**

**.**nrOfBits**(**1**),**

**.**phase**(**1**))**

Clock\_1sec **(.**clockBus**(**s\_logisimClockTree0**),**

**.**clockTick**(**s\_fpgaTick**),**

**.**globalClock**(**fpgaGlobalClock**));**

\*\* The toplevel component is connected here \*\*

main CIRCUIT\_0 **(.**AM\_PM**(**s\_AM\_PM**),**

**.**AlarmEnable**(**s\_AlarmEnable**),**

**.**D\_Mins**(**s\_D\_Mins**),**

**.**D\_hours**(**s\_D\_hours**),**

**.**D\_secs**(**s\_D\_secs**),**

**.**LoadAlarm**(**s\_LoadAlarm**),**

**.**LoadTime**(**s\_LoadTime**),**

**.**Reset**(**s\_Reset**),**

**.**logisimClockTree0**(**s\_logisimClockTree0**),**

**.**logisimOutputBubbles**(**s\_logisimOutputBubbles**));**

**endmodule**

* ClockComponent.v

**module** LogisimClockComponent**(** clockBus**,**

clockTick**,**

globalClock **);**

\*\* Here all module parameters are defined with a dummy value \*\*

**parameter** highTicks **=** 1**;**

**parameter** lowTicks **=** 1**;**

**parameter** nrOfBits **=** 1**;**

**parameter** phase **=** 1**;**

\*\* The inputs are defined here \*\*

**input** clockTick**;**

**input** globalClock**;**

\*\* The outputs are defined here \*\*

**output** **[**4**:**0**]** clockBus**;**

\*\* The wires are defined here \*\*

**wire** s\_counterIsZero**;**

**wire** **[**nrOfBits**-**1**:**0**]** s\_counterNext**;**

\*\* The registers are defined here \*\*

**reg** **[**1**:**0**]** s\_bufferRegs**;**

**reg** **[**nrOfBits**-**1**:**0**]** s\_counterValue**;**

**reg** **[**phase**-**1**:**0**]** s\_derivedClock**;**

**reg** **[**3**:**0**]** s\_outputRegs**;**

\*\* The module functionality is described here \*\*

\*\* The output signals are defined here; we synchronize them all on the main \*\*

\*\* clock \*\*

**assign** clockBus **=** **{**globalClock**,**s\_outputRegs**};**

**always** **@(posedge** globalClock**)**

**begin**

s\_bufferRegs**[**0**]** **<=** s\_derivedClock**[**phase **-** 1**];**

s\_bufferRegs**[**1**]** **<=** **~**s\_derivedClock**[**phase **-** 1**];**

s\_outputRegs**[**0**]** **<=** s\_bufferRegs**[**0**];**

s\_outputRegs**[**1**]** **<=** s\_outputRegs**[**1**];**

s\_outputRegs**[**2**]** **<=** **~**s\_bufferRegs**[**0**]** **&** s\_derivedClock**[**phase **-** 1**];**

s\_outputRegs**[**3**]** **<=** **~**s\_derivedClock**[**phase **-** 1**]** **&** s\_bufferRegs**[**0**];**

**end**

\*\* The control signals are defined here \*\*

**assign** s\_counterIsZero **=** **(**s\_counterValue **==** 0**)** **?** 1'b1 **:** 1'b0**;**

**assign** s\_counterNext **=** **(**s\_counterIsZero **==** 1'b0**)**

**?** s\_counterValue **-** 1

**:** **(**s\_derivedClock**[**0**]** **==** 1'b1**)**

**?** lowTicks **-** 1

**:** highTicks **-** 1**;**

\*\* The initial values are defined here (for simulation only) \*\*

**initial**

**begin**

s\_outputRegs **=** 0**;**

s\_derivedClock **=** 0**;**

s\_counterValue **=** 0**;**

**end**

\*\* The state registers are defined here \*\*

**integer** n**;**

**always** **@(posedge** globalClock**)**

**begin**

**if** **(**clockTick**)**

**begin**

s\_derivedClock**[**0**]** **<=** s\_derivedClock**[**0**]** **^** s\_counterIsZero**;**

**for** **(**n **=** 1**;** n **<** phase**;** n **=** n**+**1**)** **begin**

s\_derivedClock**[**n**]** **<=** s\_derivedClock**[**n**-**1**];**

**end**

**end**

**end**

**always** **@(posedge** globalClock**)**

**begin**

**if** **(**clockTick**)**

**begin**

s\_counterValue **<=** s\_counterNext**;**

**end**

**end**

**endmodule**

* TickGenrator.v

**module** logisimTickGenerator**(** FPGAClock**,**

FPGATick **);**

\*\* Here all module parameters are defined with a dummy value \*\*

**parameter** nrOfBits **=** 1**;**

**parameter** reloadValue **=** 1**;**

\*\* The inputs are defined here \*\*

**input** FPGAClock**;**

\*\* The outputs are defined here \*\*

**output** FPGATick**;**

\*\* The wires are defined here \*\*

**wire** **[**nrOfBits**-**1**:**0**]** s\_countNext**;**

**wire** s\_tickNext**;**

\*\* The registers are defined here \*\*

**reg** **[**nrOfBits**-**1**:**0**]** s\_countReg**;**

**reg** s\_tickReg**;**

\*\* The module functionality is described here \*\*

\*\* Here the output is defined \*\*

**assign** FPGATick **=** s\_tickReg**;**

\*\* Here the update logic is defined \*\*

**assign** s\_tickNext **=** **(**s\_countReg **==** 0**)** **?** 1'b1 **:** 1'b0**;**

**assign** s\_countNext **=** **(**s\_countReg **==** 0**)** **?** reloadValue**-**1 **:** s\_countReg**-**1**;**

\*\* Here the simulation only initial is defined \*\*

**initial**

**begin**

s\_countReg **=** 0**;**

s\_tickReg **=** 1'b0**;**

**end**

\*\* Here the flipflops are defined \*\*

**always** **@(posedge** FPGAClock**)**

**begin**

s\_countReg **<=** s\_countNext**;**

s\_tickReg **<=** s\_tickNext**;**

**end**

**endmodule**

* Comparator.v

**module** Comparator**(** aEqualsB**,**

aGreaterThanB**,**

aLessThanB**,**

dataA**,**

dataB **);**

\*\* Here all module parameters are defined with a dummy value \*\*

**parameter** nrOfBits **=** 1**;**

**parameter** twosComplement **=** 1**;**

\*\* The inputs are defined here \*\*

**input** **[**nrOfBits**-**1**:**0**]** dataA**;**

**input** **[**nrOfBits**-**1**:**0**]** dataB**;**

\*\* The outputs are defined here \*\*

**output** aEqualsB**;**

**output** aGreaterThanB**;**

**output** aLessThanB**;**

\*\* The wires are defined here \*\*

**wire** s\_signedGreater**;**

**wire** s\_signedLess**;**

**wire** s\_unsignedGreater**;**

**wire** s\_unsignedLess**;**

\*\* The module functionality is described here \*\*

**assign** s\_signedLess **=** **(**$signed**(**dataA**)** **<** $signed**(**dataB**));**

**assign** s\_unsignedLess **=** **(**dataA **<** dataB**);**

**assign** s\_signedGreater **=** **(**$signed**(**dataA**)** **>** $signed**(**dataB**));**

**assign** s\_unsignedGreater **=** **(**dataA **>** dataB**);**

**assign** aEqualsB **=** **(**dataA **==** dataB**);**

**assign** aGreaterThanB **=** **(**twosComplement**==**1**)** **?** s\_signedGreater **:** s\_unsignedGreater**;**

**assign** aLessThanB **=** **(**twosComplement**==**1**)** **?** s\_signedLess **:** s\_unsignedLess**;**

**endmodule**

* BCD\_to\_7seg.v

**module** BCD\_to\_7seg**(** A**,**

B**,**

C**,**

D**,**

D0**,**

D1**,**

D2**,**

D3**,**

E**,**

F**,**

G**,**

logisimClockTree0 **);**

\*\* The inputs are defined here \*\*

**input** D0**;**

**input** D1**;**

**input** D2**;**

**input** D3**;**

**input** **[**4**:**0**]** logisimClockTree0**;**

\*\* The outputs are defined here \*\*

**output** A**;**

**output** B**;**

**output** C**;**

**output** D**;**

**output** E**;**

**output** F**;**

**output** G**;**

\*\* The wires are defined here \*\*

**wire** s\_logisimNet0**;**

**wire** s\_logisimNet1**;**

**wire** s\_logisimNet10**;**

**wire** s\_logisimNet11**;**

**wire** s\_logisimNet12**;**

**wire** s\_logisimNet13**;**

**wire** s\_logisimNet14**;**

**wire** s\_logisimNet15**;**

**wire** s\_logisimNet16**;**

**wire** s\_logisimNet17**;**

**wire** s\_logisimNet18**;**

**wire** s\_logisimNet19**;**

**wire** s\_logisimNet2**;**

**wire** s\_logisimNet20**;**

**wire** s\_logisimNet21**;**

**wire** s\_logisimNet22**;**

**wire** s\_logisimNet23**;**

**wire** s\_logisimNet24**;**

**wire** s\_logisimNet25**;**

**wire** s\_logisimNet26**;**

**wire** s\_logisimNet27**;**

**wire** s\_logisimNet28**;**

**wire** s\_logisimNet29**;**

**wire** s\_logisimNet3**;**

**wire** s\_logisimNet4**;**

**wire** s\_logisimNet5**;**

**wire** s\_logisimNet6**;**

**wire** s\_logisimNet7**;**

**wire** s\_logisimNet8**;**

**wire** s\_logisimNet9**;**

\*\* The module functionality is described here \*\*

\*\* Here all input connections are defined \*\*

**assign** s\_logisimNet1 **=** D2**;**

**assign** s\_logisimNet12 **=** D3**;**

**assign** s\_logisimNet21 **=** D0**;**

**assign** s\_logisimNet6 **=** D1**;**

\*\* Here all output connections are defined \*\*

**assign** A **=** s\_logisimNet29**;**

**assign** B **=** s\_logisimNet19**;**

**assign** C **=** s\_logisimNet22**;**

**assign** D **=** s\_logisimNet3**;**

**assign** E **=** s\_logisimNet10**;**

**assign** F **=** s\_logisimNet18**;**

**assign** G **=** s\_logisimNet11**;**

\*\* Here all in-lined components are defined \*\*

// NOT Gate

**assign** s\_logisimNet4 **=** **~**s\_logisimNet6**;**

// NOT Gate

**assign** s\_logisimNet0 **=** **~**s\_logisimNet1**;**

// NOT Gate

**assign** s\_logisimNet2 **=** **~**s\_logisimNet21**;**

\*\* Here all normal components are defined \*\*

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_1 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet2**),**

**.**result**(**s\_logisimNet26**));**

OR\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_2 **(.**input1**(**s\_logisimNet17**),**

**.**input2**(**s\_logisimNet7**),**

**.**input3**(**s\_logisimNet14**),**

**.**input4**(**s\_logisimNet12**),**

**.**result**(**s\_logisimNet18**));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_3 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet2**),**

**.**result**(**s\_logisimNet8**));**

OR\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_4 **(.**input1**(**s\_logisimNet16**),**

**.**input2**(**s\_logisimNet8**),**

**.**result**(**s\_logisimNet10**));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_5 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet21**),**

**.**result**(**s\_logisimNet20**));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_6 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet4**),**

**.**result**(**s\_logisimNet25**));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_7 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet4**),**

**.**result**(**s\_logisimNet7**));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_8 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet21**),**

**.**result**(**s\_logisimNet24**));**

OR\_GATE\_3\_INPUTS **#(.**BubblesMask**(**3'b000**))**

GATES\_9 **(.**input1**(**s\_logisimNet0**),**

**.**input2**(**s\_logisimNet27**),**

**.**input3**(**s\_logisimNet24**),**

**.**result**(**s\_logisimNet19**));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_10 **(.**input1**(**s\_logisimNet0**),**

**.**input2**(**s\_logisimNet2**),**

**.**result**(**s\_logisimNet16**));**

OR\_GATE\_5\_INPUTS **#(.**BubblesMask**({**1'b0**,** 4'h0**}))**

GATES\_11 **(.**input1**(**s\_logisimNet9**),**

**.**input2**(**s\_logisimNet15**),**

**.**input3**(**s\_logisimNet5**),**

**.**input4**(**s\_logisimNet23**),**

**.**input5**(**s\_logisimNet12**),**

**.**result**(**s\_logisimNet3**));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_12 **(.**input1**(**s\_logisimNet0**),**

**.**input2**(**s\_logisimNet2**),**

**.**result**(**s\_logisimNet9**));**

OR\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_13 **(.**input1**(**s\_logisimNet13**),**

**.**input2**(**s\_logisimNet6**),**

**.**input3**(**s\_logisimNet20**),**

**.**input4**(**s\_logisimNet12**),**

**.**result**(**s\_logisimNet29**));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_14 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet2**),**

**.**result**(**s\_logisimNet23**));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_15 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet2**),**

**.**result**(**s\_logisimNet14**));**

AND\_GATE\_3\_INPUTS **#(.**BubblesMask**(**3'b000**))**

GATES\_16 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet4**),**

**.**input3**(**s\_logisimNet21**),**

**.**result**(**s\_logisimNet5**));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_17 **(.**input1**(**s\_logisimNet0**),**

**.**input2**(**s\_logisimNet6**),**

**.**result**(**s\_logisimNet28**));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_18 **(.**input1**(**s\_logisimNet0**),**

**.**input2**(**s\_logisimNet6**),**

**.**result**(**s\_logisimNet15**));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_19 **(.**input1**(**s\_logisimNet0**),**

**.**input2**(**s\_logisimNet2**),**

**.**result**(**s\_logisimNet13**));**

OR\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_20 **(.**input1**(**s\_logisimNet28**),**

**.**input2**(**s\_logisimNet25**),**

**.**input3**(**s\_logisimNet12**),**

**.**input4**(**s\_logisimNet26**),**

**.**result**(**s\_logisimNet11**));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_21 **(.**input1**(**s\_logisimNet4**),**

**.**input2**(**s\_logisimNet2**),**

**.**result**(**s\_logisimNet27**));**

OR\_GATE\_3\_INPUTS **#(.**BubblesMask**(**3'b000**))**

GATES\_22 **(.**input1**(**s\_logisimNet4**),**

**.**input2**(**s\_logisimNet21**),**

**.**input3**(**s\_logisimNet1**),**

**.**result**(**s\_logisimNet22**));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_23 **(.**input1**(**s\_logisimNet4**),**

**.**input2**(**s\_logisimNet2**),**

**.**result**(**s\_logisimNet17**));**

**endmodule**

* Bin\_to\_BCD.v

**module** Bin\_to\_BCD**(** D0**,**

D1**,**

D2**,**

D3**,**

D4**,**

D5**,**

O0**,**

O1**,**

O2**,**

O3**,**

T0**,**

T1**,**

T2**,**

T3**,**

logisimClockTree0 **);**

\*\* The inputs are defined here \*\*

**input** D0**;**

**input** D1**;**

**input** D2**;**

**input** D3**;**

**input** D4**;**

**input** D5**;**

**input** **[**4**:**0**]** logisimClockTree0**;**

\*\* The outputs are defined here \*\*

**output** O0**;**

**output** O1**;**

**output** O2**;**

**output** O3**;**

**output** T0**;**

**output** T1**;**

**output** T2**;**

**output** T3**;**

\*\* The wires are defined here \*\*

**wire** s\_logisimNet0**;**

**wire** s\_logisimNet1**;**

**wire** s\_logisimNet10**;**

**wire** s\_logisimNet11**;**

**wire** s\_logisimNet12**;**

**wire** s\_logisimNet13**;**

**wire** s\_logisimNet14**;**

**wire** s\_logisimNet15**;**

**wire** s\_logisimNet16**;**

**wire** s\_logisimNet17**;**

**wire** s\_logisimNet18**;**

**wire** s\_logisimNet19**;**

**wire** s\_logisimNet2**;**

**wire** s\_logisimNet20**;**

**wire** s\_logisimNet21**;**

**wire** s\_logisimNet22**;**

**wire** s\_logisimNet23**;**

**wire** s\_logisimNet24**;**

**wire** s\_logisimNet25**;**

**wire** s\_logisimNet26**;**

**wire** s\_logisimNet27**;**

**wire** s\_logisimNet28**;**

**wire** s\_logisimNet29**;**

**wire** s\_logisimNet3**;**

**wire** s\_logisimNet30**;**

**wire** s\_logisimNet31**;**

**wire** s\_logisimNet32**;**

**wire** s\_logisimNet33**;**

**wire** s\_logisimNet34**;**

**wire** s\_logisimNet35**;**

**wire** s\_logisimNet36**;**

**wire** s\_logisimNet37**;**

**wire** s\_logisimNet38**;**

**wire** s\_logisimNet39**;**

**wire** s\_logisimNet4**;**

**wire** s\_logisimNet40**;**

**wire** s\_logisimNet41**;**

**wire** s\_logisimNet42**;**

**wire** s\_logisimNet43**;**

**wire** s\_logisimNet44**;**

**wire** s\_logisimNet45**;**

**wire** s\_logisimNet46**;**

**wire** s\_logisimNet47**;**

**wire** s\_logisimNet48**;**

**wire** s\_logisimNet49**;**

**wire** s\_logisimNet5**;**

**wire** s\_logisimNet50**;**

**wire** s\_logisimNet51**;**

**wire** s\_logisimNet52**;**

**wire** s\_logisimNet53**;**

**wire** s\_logisimNet54**;**

**wire** s\_logisimNet55**;**

**wire** s\_logisimNet56**;**

**wire** s\_logisimNet57**;**

**wire** s\_logisimNet6**;**

**wire** s\_logisimNet7**;**

**wire** s\_logisimNet8**;**

**wire** s\_logisimNet9**;**

\*\* The module functionality is described here \*\*

\*\* Here all input connections are defined \*\*

**assign** s\_logisimNet10 **=** D3**;**

**assign** s\_logisimNet29 **=** D0**;**

**assign** s\_logisimNet3 **=** D2**;**

**assign** s\_logisimNet6 **=** D5**;**

**assign** s\_logisimNet7 **=** D4**;**

**assign** s\_logisimNet8 **=** D1**;**

\*\* Here all output connections are defined \*\*

**assign** O0 **=** s\_logisimNet35**;**

**assign** O1 **=** s\_logisimNet42**;**

**assign** O2 **=** s\_logisimNet14**;**

**assign** O3 **=** s\_logisimNet27**;**

**assign** T0 **=** s\_logisimNet33**;**

**assign** T1 **=** s\_logisimNet22**;**

**assign** T2 **=** s\_logisimNet48**;**

**assign** T3 **=** s\_logisimNet29**;**

\*\* Here all in-lined components are defined \*\*

// NOT Gate

**assign** s\_logisimNet5 **=** **~**s\_logisimNet8**;**

// NOT Gate

**assign** s\_logisimNet15 **=** **~**s\_logisimNet7**;**

// NOT Gate

**assign** s\_logisimNet0 **=** **~**s\_logisimNet3**;**

// NOT Gate

**assign** s\_logisimNet1 **=** **~**s\_logisimNet6**;**

// NOT Gate

**assign** s\_logisimNet16 **=** **~**s\_logisimNet10**;**

// Constant

**assign** s\_logisimNet35 **=** 1'b0**;**

\*\* Here all normal components are defined \*\*

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_1 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet16**),**

**.**input3**(**s\_logisimNet3**),**

**.**input4**(**s\_logisimNet5**),**

**.**result**(**s\_logisimNet34**));**

AND\_GATE\_5\_INPUTS **#(.**BubblesMask**({**1'b0**,** 4'h0**}))**

GATES\_2 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet7**),**

**.**input3**(**s\_logisimNet16**),**

**.**input4**(**s\_logisimNet3**),**

**.**input5**(**s\_logisimNet8**),**

**.**result**(**s\_logisimNet18**));**

AND\_GATE\_5\_INPUTS **#(.**BubblesMask**({**1'b0**,** 4'h0**}))**

GATES\_3 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet7**),**

**.**input3**(**s\_logisimNet16**),**

**.**input4**(**s\_logisimNet0**),**

**.**input5**(**s\_logisimNet8**),**

**.**result**(**s\_logisimNet9**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_4 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet15**),**

**.**input3**(**s\_logisimNet3**),**

**.**input4**(**s\_logisimNet5**),**

**.**result**(**s\_logisimNet44**));**

AND\_GATE\_5\_INPUTS **#(.**BubblesMask**({**1'b0**,** 4'h0**}))**

GATES\_5 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet15**),**

**.**input3**(**s\_logisimNet16**),**

**.**input4**(**s\_logisimNet3**),**

**.**input5**(**s\_logisimNet8**),**

**.**result**(**s\_logisimNet38**));**

OR\_GATE\_6\_INPUTS **#(.**BubblesMask**({**2'b00**,** 4'h0**}))**

GATES\_6 **(.**input1**(**s\_logisimNet51**),**

**.**input2**(**s\_logisimNet9**),**

**.**input3**(**s\_logisimNet38**),**

**.**input4**(**s\_logisimNet57**),**

**.**input5**(**s\_logisimNet46**),**

**.**input6**(**s\_logisimNet41**),**

**.**result**(**s\_logisimNet33**));**

AND\_GATE\_3\_INPUTS **#(.**BubblesMask**(**3'b000**))**

GATES\_7 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet16**),**

**.**input3**(**s\_logisimNet3**),**

**.**result**(**s\_logisimNet45**));**

AND\_GATE\_5\_INPUTS **#(.**BubblesMask**({**1'b0**,** 4'h0**}))**

GATES\_8 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet7**),**

**.**input3**(**s\_logisimNet10**),**

**.**input4**(**s\_logisimNet3**),**

**.**input5**(**s\_logisimNet5**),**

**.**result**(**s\_logisimNet41**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_9 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet15**),**

**.**input3**(**s\_logisimNet10**),**

**.**input4**(**s\_logisimNet8**),**

**.**result**(**s\_logisimNet19**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_10 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet15**),**

**.**input3**(**s\_logisimNet10**),**

**.**input4**(**s\_logisimNet8**),**

**.**result**(**s\_logisimNet26**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_11 **(.**input1**(**s\_logisimNet15**),**

**.**input2**(**s\_logisimNet16**),**

**.**input3**(**s\_logisimNet3**),**

**.**input4**(**s\_logisimNet5**),**

**.**result**(**s\_logisimNet2**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_12 **(.**input1**(**s\_logisimNet7**),**

**.**input2**(**s\_logisimNet10**),**

**.**input3**(**s\_logisimNet0**),**

**.**input4**(**s\_logisimNet5**),**

**.**result**(**s\_logisimNet40**));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_13 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet10**),**

**.**result**(**s\_logisimNet12**));**

AND\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_14 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet7**),**

**.**result**(**s\_logisimNet20**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_15 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet7**),**

**.**input3**(**s\_logisimNet10**),**

**.**input4**(**s\_logisimNet0**),**

**.**result**(**s\_logisimNet30**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_16 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet15**),**

**.**input3**(**s\_logisimNet10**),**

**.**input4**(**s\_logisimNet3**),**

**.**result**(**s\_logisimNet43**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_17 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet10**),**

**.**input3**(**s\_logisimNet3**),**

**.**input4**(**s\_logisimNet8**),**

**.**result**(**s\_logisimNet50**));**

OR\_GATE\_8\_INPUTS **#(.**BubblesMask**(**8'h00**))**

GATES\_18 **(.**input1**(**s\_logisimNet19**),**

**.**input2**(**s\_logisimNet53**),**

**.**input3**(**s\_logisimNet55**),**

**.**input4**(**s\_logisimNet50**),**

**.**input5**(**s\_logisimNet25**),**

**.**input6**(**s\_logisimNet45**),**

**.**input7**(**s\_logisimNet54**),**

**.**input8**(**s\_logisimNet4**),**

**.**result**(**s\_logisimNet27**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_19 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet7**),**

**.**input3**(**s\_logisimNet0**),**

**.**input4**(**s\_logisimNet5**),**

**.**result**(**s\_logisimNet52**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_20 **(.**input1**(**s\_logisimNet7**),**

**.**input2**(**s\_logisimNet16**),**

**.**input3**(**s\_logisimNet0**),**

**.**input4**(**s\_logisimNet8**),**

**.**result**(**s\_logisimNet4**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_21 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet7**),**

**.**input3**(**s\_logisimNet10**),**

**.**input4**(**s\_logisimNet0**),**

**.**result**(**s\_logisimNet54**));**

OR\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_22 **(.**input1**(**s\_logisimNet24**),**

**.**input2**(**s\_logisimNet11**),**

**.**input3**(**s\_logisimNet56**),**

**.**input4**(**s\_logisimNet47**),**

**.**result**(**s\_logisimNet14**));**

AND\_GATE\_3\_INPUTS **#(.**BubblesMask**(**3'b000**))**

GATES\_23 **(.**input1**(**s\_logisimNet7**),**

**.**input2**(**s\_logisimNet10**),**

**.**input3**(**s\_logisimNet3**),**

**.**result**(**s\_logisimNet47**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_24 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet15**),**

**.**input3**(**s\_logisimNet16**),**

**.**input4**(**s\_logisimNet5**),**

**.**result**(**s\_logisimNet21**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_25 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet15**),**

**.**input3**(**s\_logisimNet16**),**

**.**input4**(**s\_logisimNet3**),**

**.**result**(**s\_logisimNet37**));**

AND\_GATE\_5\_INPUTS **#(.**BubblesMask**({**1'b0**,** 4'h0**}))**

GATES\_26 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet7**),**

**.**input3**(**s\_logisimNet10**),**

**.**input4**(**s\_logisimNet0**),**

**.**input5**(**s\_logisimNet5**),**

**.**result**(**s\_logisimNet36**));**

AND\_GATE\_5\_INPUTS **#(.**BubblesMask**({**1'b0**,** 4'h0**}))**

GATES\_27 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet7**),**

**.**input3**(**s\_logisimNet16**),**

**.**input4**(**s\_logisimNet0**),**

**.**input5**(**s\_logisimNet5**),**

**.**result**(**s\_logisimNet39**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_28 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet7**),**

**.**input3**(**s\_logisimNet16**),**

**.**input4**(**s\_logisimNet0**),**

**.**result**(**s\_logisimNet55**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_29 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet15**),**

**.**input3**(**s\_logisimNet16**),**

**.**input4**(**s\_logisimNet8**),**

**.**result**(**s\_logisimNet17**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_30 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet16**),**

**.**input3**(**s\_logisimNet3**),**

**.**input4**(**s\_logisimNet8**),**

**.**result**(**s\_logisimNet28**));**

AND\_GATE\_5\_INPUTS **#(.**BubblesMask**({**1'b0**,** 4'h0**}))**

GATES\_31 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet15**),**

**.**input3**(**s\_logisimNet10**),**

**.**input4**(**s\_logisimNet0**),**

**.**input5**(**s\_logisimNet5**),**

**.**result**(**s\_logisimNet57**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_32 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet15**),**

**.**input3**(**s\_logisimNet10**),**

**.**input4**(**s\_logisimNet3**),**

**.**result**(**s\_logisimNet53**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_33 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet10**),**

**.**input3**(**s\_logisimNet3**),**

**.**input4**(**s\_logisimNet8**),**

**.**result**(**s\_logisimNet32**));**

AND\_GATE\_3\_INPUTS **#(.**BubblesMask**(**3'b000**))**

GATES\_34 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet7**),**

**.**input3**(**s\_logisimNet3**),**

**.**result**(**s\_logisimNet11**));**

OR\_GATE **#(.**BubblesMask**(**2'b00**))**

GATES\_35 **(.**input1**(**s\_logisimNet12**),**

**.**input2**(**s\_logisimNet20**),**

**.**result**(**s\_logisimNet42**));**

OR\_GATE\_10\_INPUTS **#(.**BubblesMask**({**2'b00**,** 8'h00**}))**

GATES\_36 **(.**input1**(**s\_logisimNet31**),**

**.**input10**(**s\_logisimNet43**),**

**.**input2**(**s\_logisimNet52**),**

**.**input3**(**s\_logisimNet18**),**

**.**input4**(**s\_logisimNet40**),**

**.**input5**(**s\_logisimNet30**),**

**.**input6**(**s\_logisimNet2**),**

**.**input7**(**s\_logisimNet37**),**

**.**input8**(**s\_logisimNet44**),**

**.**input9**(**s\_logisimNet23**),**

**.**result**(**s\_logisimNet22**));**

AND\_GATE\_3\_INPUTS **#(.**BubblesMask**(**3'b000**))**

GATES\_37 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet15**),**

**.**input3**(**s\_logisimNet16**),**

**.**result**(**s\_logisimNet25**));**

AND\_GATE\_4\_INPUTS **#(.**BubblesMask**(**4'h0**))**

GATES\_38 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet15**),**

**.**input3**(**s\_logisimNet3**),**

**.**input4**(**s\_logisimNet8**),**

**.**result**(**s\_logisimNet23**));**

AND\_GATE\_5\_INPUTS **#(.**BubblesMask**({**1'b0**,** 4'h0**}))**

GATES\_39 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet7**),**

**.**input3**(**s\_logisimNet16**),**

**.**input4**(**s\_logisimNet0**),**

**.**input5**(**s\_logisimNet5**),**

**.**result**(**s\_logisimNet51**));**

OR\_GATE\_10\_INPUTS **#(.**BubblesMask**({**2'b00**,** 8'h00**}))**

GATES\_40 **(.**input1**(**s\_logisimNet17**),**

**.**input10**(**s\_logisimNet32**),**

**.**input2**(**s\_logisimNet49**),**

**.**input3**(**s\_logisimNet39**),**

**.**input4**(**s\_logisimNet28**),**

**.**input5**(**s\_logisimNet13**),**

**.**input6**(**s\_logisimNet21**),**

**.**input7**(**s\_logisimNet26**),**

**.**input8**(**s\_logisimNet34**),**

**.**input9**(**s\_logisimNet36**),**

**.**result**(**s\_logisimNet48**));**

AND\_GATE\_3\_INPUTS **#(.**BubblesMask**(**3'b000**))**

GATES\_41 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet7**),**

**.**input3**(**s\_logisimNet10**),**

**.**result**(**s\_logisimNet56**));**

AND\_GATE\_5\_INPUTS **#(.**BubblesMask**({**1'b0**,** 4'h0**}))**

GATES\_42 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet7**),**

**.**input3**(**s\_logisimNet10**),**

**.**input4**(**s\_logisimNet0**),**

**.**input5**(**s\_logisimNet8**),**

**.**result**(**s\_logisimNet46**));**

AND\_GATE\_3\_INPUTS **#(.**BubblesMask**(**3'b000**))**

GATES\_43 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet15**),**

**.**input3**(**s\_logisimNet16**),**

**.**result**(**s\_logisimNet24**));**

AND\_GATE\_5\_INPUTS **#(.**BubblesMask**({**1'b0**,** 4'h0**}))**

GATES\_44 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet15**),**

**.**input3**(**s\_logisimNet10**),**

**.**input4**(**s\_logisimNet3**),**

**.**input5**(**s\_logisimNet5**),**

**.**result**(**s\_logisimNet49**));**

AND\_GATE\_5\_INPUTS **#(.**BubblesMask**({**1'b0**,** 4'h0**}))**

GATES\_45 **(.**input1**(**s\_logisimNet1**),**

**.**input2**(**s\_logisimNet7**),**

**.**input3**(**s\_logisimNet10**),**

**.**input4**(**s\_logisimNet0**),**

**.**input5**(**s\_logisimNet8**),**

**.**result**(**s\_logisimNet13**));**

AND\_GATE\_5\_INPUTS **#(.**BubblesMask**({**1'b0**,** 4'h0**}))**

GATES\_46 **(.**input1**(**s\_logisimNet6**),**

**.**input2**(**s\_logisimNet15**),**

**.**input3**(**s\_logisimNet16**),**

**.**input4**(**s\_logisimNet0**),**

**.**input5**(**s\_logisimNet8**),**

**.**result**(**s\_logisimNet31**));**

**endmodule**

* And\_gate\_5\_inputs.v

**module** AND\_GATE\_5\_INPUTS**(** input1**,**

input2**,**

input3**,**

input4**,**

input5**,**

result **);**

\*\* Here all module parameters are defined with a dummy value \*\*

**parameter** **[**64**:**0**]** BubblesMask **=** 1**;**

\*\* The inputs are defined here \*\*

**input** input1**;**

**input** input2**;**

**input** input3**;**

**input** input4**;**

**input** input5**;**

\*\* The outputs are defined here \*\*

**output** result**;**

\*\* The wires are defined here \*\*

**wire** s\_realInput2**;**

**wire** s\_realInput3**;**

**wire** s\_realInput4**;**

**wire** s\_realInput5**;**

\*\* The module functionality is described here \*\*

\*\* Here the bubbles are processed \*\*

**assign** s\_realInput1 **=** **(**BubblesMask**[**0**]** **==** 1'b0**)** **?** input1 **:** **~**input1**;**

**assign** s\_realInput2 **=** **(**BubblesMask**[**1**]** **==** 1'b0**)** **?** input2 **:** **~**input2**;**

**assign** s\_realInput3 **=** **(**BubblesMask**[**2**]** **==** 1'b0**)** **?** input3 **:** **~**input3**;**

**assign** s\_realInput4 **=** **(**BubblesMask**[**3**]** **==** 1'b0**)** **?** input4 **:** **~**input4**;**

**assign** s\_realInput5 **=** **(**BubblesMask**[**4**]** **==** 1'b0**)** **?** input5 **:** **~**input5**;**

\*\* Here the functionality is defined \*\*

**assign** result **=** s\_realInput1**&**

s\_realInput2**&**

s\_realInput3**&**

s\_realInput4**&**

s\_realInput5**;**

**endmodule**

* Or\_gate\_5\_inputs.v

**module** OR\_GATE\_5\_INPUTS**(** input1**,**

input2**,**

input3**,**

input4**,**

input5**,**

result **);**

\*\* Here all module parameters are defined with a dummy value \*\*

**parameter** **[**64**:**0**]** BubblesMask **=** 1**;**

\*\* The inputs are defined here \*\*

**input** input1**;**

**input** input2**;**

**input** input3**;**

**input** input4**;**

**input** input5**;**

\*\* The outputs are defined here \*\*

**output** result**;**

\*\* The wires are defined here \*\*

**wire** s\_realInput1**;**

**wire** s\_realInput2**;**

**wire** s\_realInput3**;**

**wire** s\_realInput4**;**

**wire** s\_realInput5**;**

\*\* The module functionality is described here \*\*

\*\* Here the bubbles are processed \*\*

**assign** s\_realInput1 **=** **(**BubblesMask**[**0**]** **==** 1'b0**)** **?** input1 **:** **~**input1**;**

**assign** s\_realInput2 **=** **(**BubblesMask**[**1**]** **==** 1'b0**)** **?** input2 **:** **~**input2**;**

**assign** s\_realInput3 **=** **(**BubblesMask**[**2**]** **==** 1'b0**)** **?** input3 **:** **~**input3**;**

**assign** s\_realInput4 **=** **(**BubblesMask**[**3**]** **==** 1'b0**)** **?** input4 **:** **~**input4**;**

**assign** s\_realInput5 **=** **(**BubblesMask**[**4**]** **==** 1'b0**)** **?** input5 **:** **~**input5**;**

\*\* Here the functionality is defined \*\*

**assign** result **=** s\_realInput1**|**

s\_realInput2**|**

s\_realInput3**|**

s\_realInput4**|**

s\_realInput5**;**

**endmodule**

* D\_FLIPFLOP.v

**module** D\_FLIPFLOP**(** clock**,**

d**,**

preset**,**

q**,**

qBar**,**

reset**,**

tick **);**

\*\* Here all module parameters are defined with a dummy value \*\*

**parameter** invertClockEnable **=** 1**;**

\*\* The inputs are defined here \*\*

**input** clock**;**

**input** d**;**

**input** preset**;**

**input** reset**;**

**input** tick**;**

\*\* The outputs are defined here \*\*

**output** q**;**

**output** qBar**;**

\*\* The wires are defined here \*\*

**wire** s\_clock**;**

**wire** s\_nextState**;**

\*\* The registers are defined here \*\*

**reg** s\_currentState**;**

\*\* The module functionality is described here \*\*

\*\* Here the output signals are defined \*\*

**assign** q **=** s\_currentState**;**

**assign** qBar **=** **~(**s\_currentState**);**

**assign** s\_clock **=** **(**invertClockEnable **==** 0**)** **?** clock **:** **~**clock**;**

\*\* Here the initial register value is defined; for simulation only \*\*

**initial**

**begin**

s\_currentState **=** 0**;**

**end**

\*\* Here the update logic is defined \*\*

**assign** s\_nextState **=** d**;**

\*\* Here the actual state register is defined \*\*

**always** **@(posedge** reset **or** **posedge** preset **or** **posedge** s\_clock**)**

**begin**

**if** **(**reset**)** s\_currentState **<=** 1'b0**;**

**else** **if** **(**preset**)** s\_currentState **<=** 1'b1**;**

**else** **if** **(**tick**)** s\_currentState **<=** s\_nextState**;**

**end**

**endmodule**

* Counter.v

**module** LogisimCounter**(** clear**,**

clock**,**

compareOut**,**

countValue**,**

enable**,**

load**,**

loadData**,**

tick**,**

upNotDown **);**

\*\* Here all module parameters are defined with a dummy value \*\*

**parameter** **[**64**:**0**]** maxVal **=** 1**;**

**parameter** invertClock **=** 1**;**

**parameter** mode **=** 1**;**

**parameter** width **=** 1**;**

\*\* The inputs are defined here \*\*

**input** clear**;**

**input** clock**;**

**input** enable**;**

**input** load**;**

**input** **[**width**-**1**:**0**]** loadData**;**

**input** tick**;**

**input** upNotDown**;**

\*\* The outputs are defined here \*\*

**output** compareOut**;**

**output** **[**width**-**1**:**0**]** countValue**;**

\*\* The wires are defined here \*\*

**wire** s\_clock**;**

**wire** s\_realEnable**;**

\*\* The registers are defined here \*\*

**reg** s\_carry**;**

**reg** **[**width**-**1**:**0**]** s\_counterValue**;**

**reg** **[**width**-**1**:**0**]** s\_nextCounterValue**;**

\*\* The module functionality is described here \*\*

\*\* Functionality of the counter: \*\*

\*\* Load Count | mode \*\*

\*\* \*\*

\*\* -----------+------------------- \*\*

\*\* 0 0 | halt \*\*

\*\* 0 1 | count \*\*

\*\* up (default) \*\*

\*\* 1 0 | load \*\*

\*\* 1 1 | count down \*\*

**assign** compareOut **=** s\_carry**;**

**assign** countValue **=** s\_counterValue**;**

**assign** s\_clock **=** **(**invertClock **==** 0**)** **?** clock **:** **~**clock**;**

**always@(\*)**

**begin**

**if** **(**upNotDown**)**

s\_carry **=** **(**s\_counterValue **==** maxVal**)** **?** 1'b1 **:** 1'b0**;**

**else**

s\_carry **=** **(**s\_counterValue **==** 0**)** **?** 1'b1 **:** 1'b0**;**

**end**

**assign** s\_realEnable **=** **((~(**load**)&~(**enable**))|**

**((**mode**==**1**)&**s\_carry**&~(**load**)))** **?** 1'b0 **:** tick**;**

**always** **@(\*)**

**begin**

**if** **((**load**)|((**mode**==**3**)&**s\_carry**))**

s\_nextCounterValue **=** loadData**;**

**else** **if** **((**mode**==**0**)&**s\_carry**&**upNotDown**)**

s\_nextCounterValue **=** 0**;**

**else** **if** **((**mode**==**0**)&**s\_carry**)**

s\_nextCounterValue **=** maxVal**;**

**else** **if** **(**upNotDown**)**

s\_nextCounterValue **=** s\_counterValue **+** 1**;**

**else**

s\_nextCounterValue **=** s\_counterValue **-** 1**;**

**end**

**always** **@(posedge** s\_clock **or** **posedge** clear**)**

**begin**

**if** **(**clear**)** s\_counterValue **<=** 0**;**

**else** **if** **(**s\_realEnable**)** s\_counterValue **<=** s\_nextCounterValue**;**

**end**

**endmodule**

* REGISTER\_FLIP\_FLOP.v

**module** REGISTER\_FLIP\_FLOP**(** clock**,**

clockEnable**,**

d**,**

q**,**

reset**,**

tick **);**

\*\* Here all module parameters are defined with a dummy value \*\*

**parameter** invertClock **=** 1**;**

**parameter** nrOfBits **=** 1**;**

\*\* The inputs are defined here \*\*

**input** clock**;**

**input** clockEnable**;**

**input** **[**nrOfBits**-**1**:**0**]** d**;**

**input** reset**;**

**input** tick**;**

\*\* The outputs are defined here \*\*

**output** **[**nrOfBits**-**1**:**0**]** q**;**

\*\* The wires are defined here \*\*

**wire** s\_clock**;**

\*\* The registers are defined here \*\*

**reg** **[**nrOfBits**-**1**:**0**]** s\_currentState**;**

\*\* The module functionality is described here \*\*

**assign** q **=** s\_currentState**;**

**assign** s\_clock **=** invertClock **==** 0 **?** clock **:** **~**clock**;**

**always** **@(posedge** s\_clock **or** **posedge** reset**)**

**begin**

**if** **(**reset**)** s\_currentState **<=** 0**;**

**else** **if** **(**clockEnable**&**tick**)** s\_currentState **<=** d**;**

**end**

**endmodule**

* Multiplexer\_bus\_4.v

**module** Multiplexer\_bus\_4**(** enable**,**

muxIn\_0**,**

muxIn\_1**,**

muxIn\_2**,**

muxIn\_3**,**

muxOut**,**

sel **);**

\*\* Here all module parameters are defined with a dummy value \*\*

**parameter** nrOfBits **=** 1**;**

\*\* The inputs are defined here \*\*

**input** enable**;**

**input** **[**nrOfBits**-**1**:**0**]** muxIn\_0**;**

**input** **[**nrOfBits**-**1**:**0**]** muxIn\_1**;**

**input** **[**nrOfBits**-**1**:**0**]** muxIn\_2**;**

**input** **[**nrOfBits**-**1**:**0**]** muxIn\_3**;**

**input** **[**1**:**0**]** sel**;**

\*\* The outputs are defined here \*\*

**output** **[**nrOfBits**-**1**:**0**]** muxOut**;**

\*\* The module functionality is described here \*\*

**reg** **[**nrOfBits**:**0**]** s\_selected\_vector**;**

**assign** muxOut **=** s\_selected\_vector**;**

**always** **@(\*)**

**begin**

**if** **(~**enable**)** s\_selected\_vector **<=** 0**;**

**else** **case** **(**sel**)**

2'b00**:**

s\_selected\_vector **<=** muxIn\_0**;**

2'b01**:**

s\_selected\_vector **<=** muxIn\_1**;**

2'b10**:**

s\_selected\_vector **<=** muxIn\_2**;**

**default:**

s\_selected\_vector **<=** muxIn\_3**;**

**endcase**

**end**

**endmodule**

* Priority\_Encode.v

**module** priority\_encoder**(**A0**,**A1**,**Y0**,**Y1**,**Y2**,**Y3**);**

**input** Y3**,** Y2**,** Y1**,** Y0**;**

**output** A0**,** A1**;**

**assign** A0 **=** **(**Y3**)** **?** 1 **:**

**(**Y2**)** **?** 1 **:**

**(**Y1**)** **?** 0 **:**

**(**Y0**)** **?** 0 **:** 1'b0**;**

**assign** A1 **=(**Y3**)** **?** 1 **:**

**(**Y2**)** **?** 0 **:**

**(**Y1**)** **?** 1 **:**

**(**Y0**)** **?** 0 **:** 1'b0**;**

**endmodule**